Minimizing Clock Induced Charge

Clock Induced Charge (CIC) can be considered the remaining detection limit in EMCCD and must be minimized. Careful and rapid clocking are crucial contributors to achieving this.

The remaining limiting factor for EMCCD sensitivity, provided darkcurrent has already been minimized through effective TE cooling, is a spurious noise source called Clock Induced Charge (CIC). This form of electron generation can occur even under normal clocking in any CCD, but when properly optimized the rate of occurrence is very small; i.e. CIC occurrence can be minimized down to the order of 1 in 200 pixels. For an EMCCD at high EM gain, such individual electrons can be seen as sharp spikes in the image and any CIC will become visible.

For several years, Andor have had very fine nanosecond resolution over EMCCD clockings and are well aware of the important parameters for reducing CIC, such as fine temporal control over the clock edges. Furthermore, there is a well-established direct link between pushing vertical clocks faster and achieving lower CIC. This clock speed dependence is amply illustrated in the following basic test:

Figure 1 shows a series of dark images and corresponding intensity profiles (across a random row from each image), using 30 ms exposures and EM gain of x1000. The cooling temperature in each case was set at -85°C to ensure virtual elimination of darkcurrent contribution, so any amplified noise spikes are derived primarily from the remaining CIC.

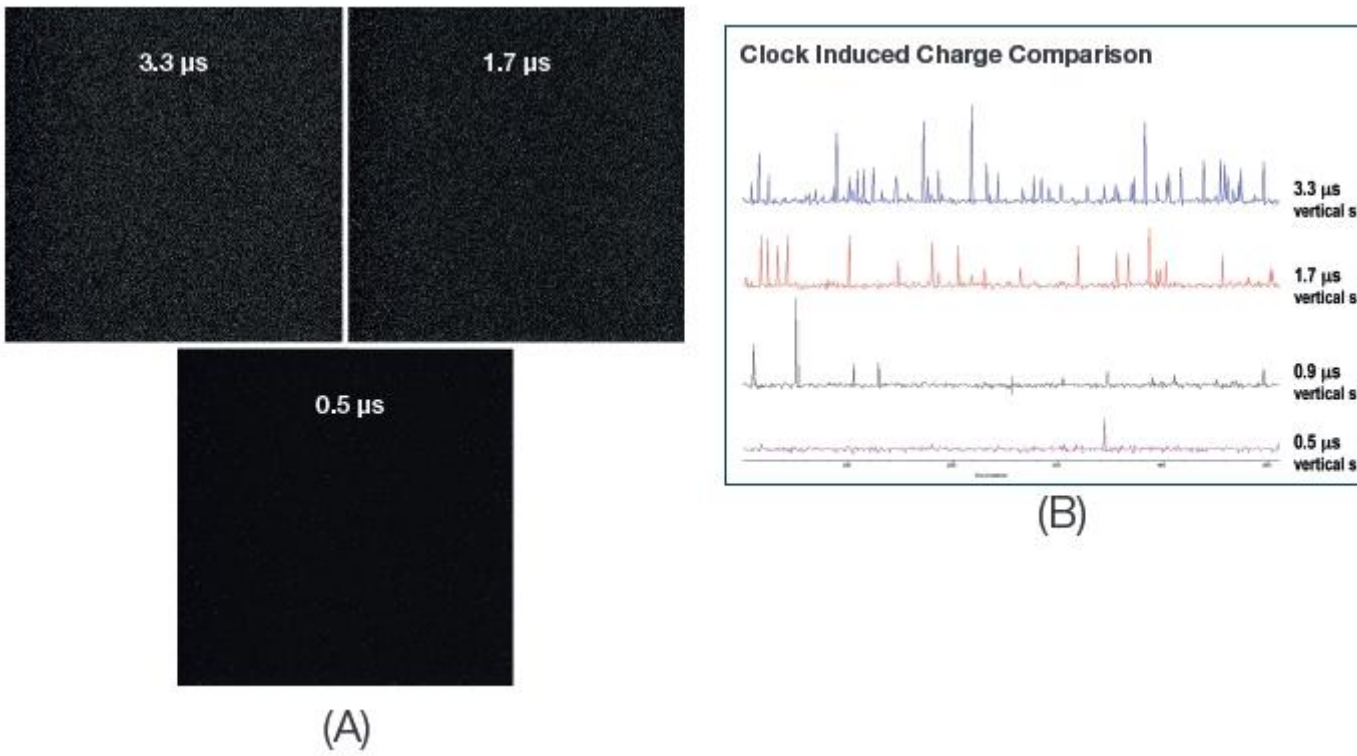

Figure 1 - (A) shows DARK IMAGES taken at x1000 gain at different vertical shift speeds, 29 ms exposure time. Cooling temperature was -85°C to ensure minimal darkcurrent contribution. **(B)** shows typical line intensity profiles across a row of 512 pixels, taken from such dark images at three different vertical shift speeds. The cleanest noise floor is clearly seen under conditions of faster vertical shifts, an exclusive Andor capability.

You can see that the vertical clock speeds have a significant impact on further reducing CIC, with the speed of 0.5 µs/shift offering the lowest CIC and therefore highest EMCCD sensitivity. This iXon3 clock speed performance is faster than other EMCCDs in the industry.

After having minimized darkcurrent through < -80°C cooling, the remaining detection limit in back-illuminated EMCCDs is given by the number of Clock-Induced Charge noise events.

Andor's industry-exclusive combination of high resolution clocking parameters and sub-microsecond clock speeds are fundamental to minimizing CIC, enabling truly 'high-end' EMCCD sensitivity to be claimed.