DATA SHEET

M8132A – 640 Gb/s Digital Signal Processor

Version 2.1, November 2020

KEYSIGHT TECHNOLOGIES

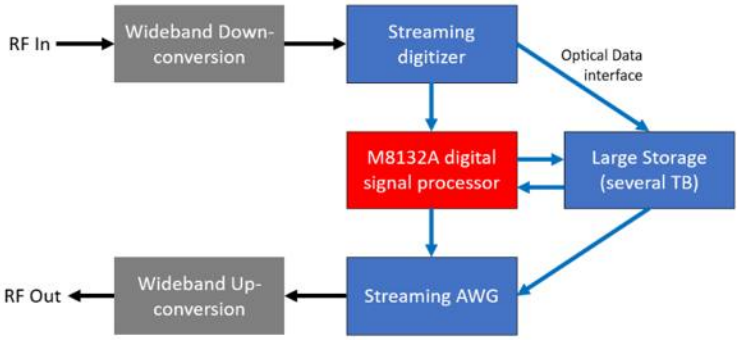
M8132A at a glance

Key features

- Two large Xilinx Ultrascale+ VU9P FPGAs available for custom processing functions
- 4 x 160 Gb/s bidirectional optical data interfaces (ODI) or 3 x ODI + 8 x 10 GbE interfaces
- Aggregate throughput up to 640 Gb/s input + 640 Gb/s output
- PCIe backplane interface up to Gen3 x8
- Deterministic latency between Digitizer, DSP module and AWG
- 2-slot AXIe module
- Part of Keysight's Wideband Solution Platform (WSP).

Wideband Solution Platform

The M8132A is part of Keysight's Wideband Solution Platform that consists of a portfolio of compatible instruments, including digitizer, arbitrary waveform generator, digital signal processor and storage modules. The interconnect between these products is based on a high-speed optical data interface.



Optical Data Interface / Gigabit Ethernet Interface

The AXIe Consortium has standardized a high-speed optical data interface (ODI) for advanced instrumentation and embedded systems (http://www.axiestandard.org/odispecifications.html).

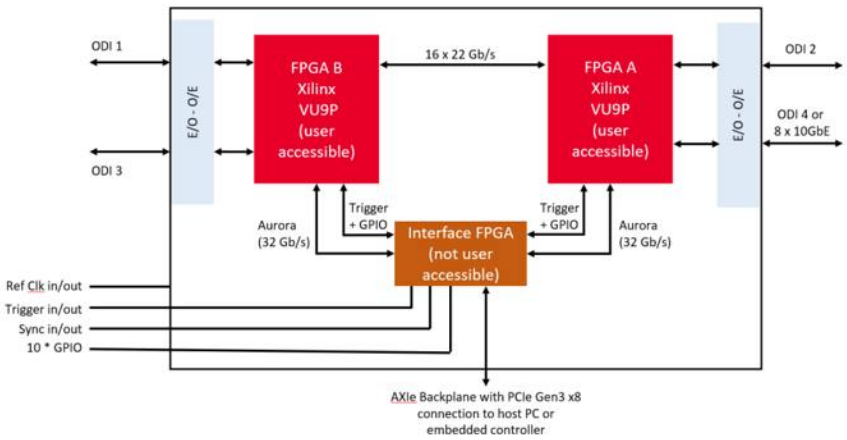
The M8132A has four ODI ports on the front panel, each of which allows digital data to be transmitted and received at up to 160 Gb/s per direction.

The optical data interface serves as a backbone between wideband digitizers, AWGs, digital signal processing modules, mass storage devices or custom hardware. Due to the modular structure, different system configurations can be realized. A few examples are shown in the Applications section below.

One of the ODI interfaces can alternatively be configured as eight 10 Gigabit Ethernet (10 GbE) interfaces, as shown in the following system block diagram.

System Block diagram

The M8132A is a powerful digital signal processing engine consisting of two Xilinx Ultrascale+ VU9P FPGAs, four ODI interfaces running at up to 160 Gb/s in+out each,



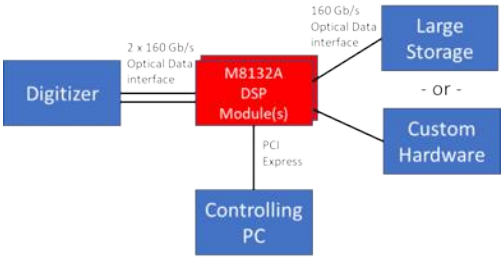
an inter-FPGA link that consists of 16 high-speed links at up to 22 Gb/s and a PCIe Gen3 x8 link to the AXIe backplane. In addition, the module provides a trigger input and output, synchronization input and outputs for deterministic latency between compatible digitizers and AWG modules as well as 10 general purpose I/Os.

Applications

Two large FPGAs provide endless signal processing and generation possibilities. Here are a few examples.

Real-time processing of captured data

In many cases, captured data from a digitizer needs to be post-processed in real-time. This can be accomplished in one or more M8132A DSP modules. Possible applications include:

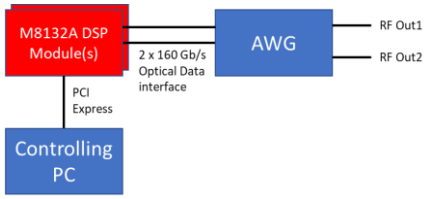


- Demodulation of a communications signal
- Protocol analysis
- Pulse-descriptor-word extraction from a received radar signal
- Real-time spectrum analysis
- Determination of the angle-of-arrival in a phased array antenna
- Custom digital signal processing

Depending on the bandwidth of the post-processed data, it can be streamed into a compatible mass storage device or into other custom hardware for further processing.

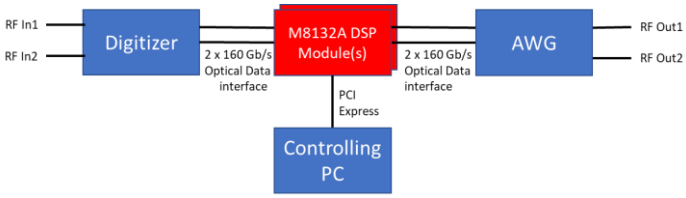
Realtime signal generation

In some AWG applications, waveforms and sequences are too complex to store them in the memory of a conventional AWG. The M8132A can offer a possibility to calculate the AWG waveform in real-time, e.g. radar pulses based on pulse descriptor words or a radio signal based on the digital content



Record and Playback

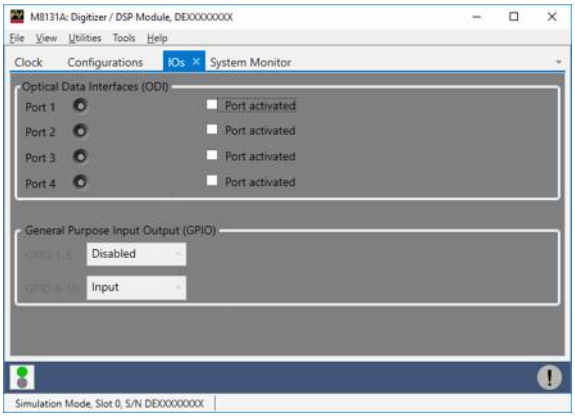
In combination with a compatible AWG and digitizer, the M8132A can perform real-time processing in a wideband record and playback system. Depending on the amount of processing required, one or more M8132A modules can be cascaded.



Software

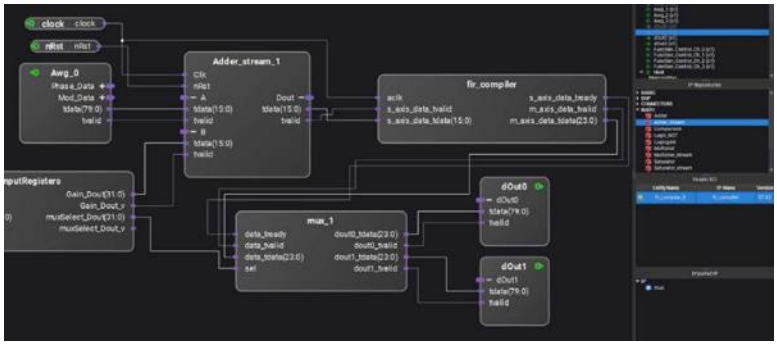
The M8132A is controlled from a windows-based PC through PCI Express or USB. A soft front panel application contains the necessary functions for configuring the ODI ports and loading FPGA images.

The soft front panel application also provides a SCPI interface for controlling the M8132A remotely.



FPGA Design and Configuration

Keysight offers the KF9000A PathWave FPGA Programming Environment that allows users to design and configure the FPGAs inside the M8132A. Please refer to http://www.keysight.com/find/pathwave-fpga for further information.



Board Support Package

The M8132A software includes a board support package (BSP). The BSP is the interface between the PathwaveFPGA software and the hardware and FPGA resources that are available in the M8132A. The BSP can be instantiated in two different configurations:

a) 4 ODI ports (2 ODI ports per FPGA)

b) 3 ODI ports + 8 10GbE ports (FPGA A: 1 ODI port and 8 10GbE ports; FPGA B: 2 ODI ports)

The inter-FPGA link, trigger and general purpose I/Os are available in both configurations.

A detailed list of available resources in each of the FPGAs is described below.

Since the BSP contains licensed IP from Xilinx, customers are required to agree to an EULA amendment before they can access the BSP code. Please contact Keysight if you want to review this EULA amendment before purchasing the M8132A.

Description	Product #	Comment
640 Gb/s digital signal processor module with 2 user accessible FPGAs	M8132A-002	The DSP module comes with two 1m ODI cables. Additional ODI cables can be ordered under M8131A-831 or M8131A-833
Pathwave FPGA Software	KF9000A	See KF9000A datasheet for licensing details
GPIO cable	8121-4100	MPN: FCF8-10-01 from Samtec
ODI to 10GbE cable	M8132A-830	Adapter cable for ODI to 8 x 10GbE
Optical Data Interface cable, 1 m	M8131A-831	No ODI cables are included. Please order the desired number of cables separately
Optical Data Interface cable, 3 m	M8131A-833	
AXIe infrastructure:		
2-slot AXIe chassis with USB option	M9502A-U20	PCIe x8 Gen 2 and USB
5-slot AXIe chassis with USB option	M9505A-U20	PCIe x8 Gen 2 and USB
5-slot AXIe chassis	M9506A	PCIe x8 Gen 3 and Thunderbolt
PCIe desktop card adapter x8 Gen 2	M9048A	
PCIe desktop card adapter x8 Gen 3	M9048B	
PCIe desktop card adapter dual port x16 Gen 3	M9049A	
x8 – x8 PCIe cable	Y1202A	
Embedded AXIe controller	M9537A	

Performance Characteristics

User accessible FPGAs

FPGA type	2 x Xilinx UltraScale+ VU9P, speed grade -2	
Total available CLB Flip-Flops (k)	2364 for FPGA A	+ 2364 for FPGA B
Total available CLB LUT (k)	1182 for FPGA A	+ 1182 for FPGA B
Total available Max Dist. RAM (Mb)	36.1 for FPGA A	+ 36.1 for FPGA B
Total available Block RAM (Mb)	75.9 for FPGA A	+ 75.9 for FPGA B
Total available Ultra RAM (Mb)	270 for FPGA A	+ 270 for FPGA B
Total available Clock Mgmt Tiles (CMT)	30 for FPGA A	+ 30 for FPGA B
Total available DSP Slices	6840 for FPGA A	+ 6840 for FPGA B
Total available Global Buffers	1800 for FPGA A	+ 1800 for FPGA B

Board Support Package

The following resources are available in the customer accessible region of each of the two FPGAs. The same amount of resources is available for both configurations of the BSP (4 x ODI and 3 x ODI + 8 x 10GbE)

Xilinx Vivado Design Suite	Version 2019.2 (or later)	
Keysight KF9000A PathWave FPGA Programming Environment	Version 2020 Update 1 (or later)	
	FPGA A (both configurations)	**FPGA B**
CLB Flip-Flops (k)	1584 (68% of total)	1530 (66% of total)
CLB LUT (k)	792 (68% of total)	765 (66% of total)
Max Dist. RAM (Mb)	24.8 (72% of total)	23.9 (69% of total)
Total Block RAM (Mb)	50.625 (66% of total)	48.1 (63% of total)
UltraRAM (Mb)	229.5 (85% of total)	225 (83% of total)
Clock Mgmt Tiles (CMTs)	62 (69% of total)	60 (67% of total)
DSP Slices	4848 (71% of total)	4224 (62% of total)
Global Buffers	1020 (56% of total)	1032 (57% of total)
Optical interfaces	ODI 2 + ODI 4 or ODI 2 + 8 x 10GbE	ODI 1 + ODI 3
Inter-FPGA link	Max. throughput 16 x 22 Gb/s. Available throughput is lower, due to protocol overhead	
Trigger Out	see section "Trigger Out" below	
Trigger In + 5 x GP inputs	Connected to 3 inputs per FPGA via switch matrix	
5 x GP outputs	Connected to 3 outputs per FPGA via switch matrix	
Deterministic latency	Supported (ODI1 to ODI3)	Supported (ODI2 to ODI4)

Optical Data Interfaces

Number of ODI ports	4 (2 ODI ports per FPGA) – see BSP above
Lane rate	12 x 14.1 Gb/s per direction per ODI connector
Supported data formats	User defined
Supported packet formats	User defined
Supported burst sizes	User defined
Flow control	User defined
Connector type	MPO 24

Trigger In

A trigger input is provided on the front panel. This signal can be routed to FPGA A or FPGA B via switch matrix.

Input range	-4 to +4 V
Threshold	
Range	-4 to +4 V
Resolution	10 mV (nom.)
Sensitivity	100 mV (typ.)
Polarity	Positive
Input impedance	50 Ω (nom.), DC coupled
Max toggle frequency	50 MHz (nom.)
Minimum pulse width	5 ns (nom.)
Minimum inactive time	5 ns (nom.)
Connector	SMA

Trigger Out

A trigger output is provided on the front panel. This signal can be configured to output a static “low”, a static “high”, a 50% toggle (200 MHz) or a user generated output signal from the BSP, sourced from either FPGA A or FPGA B.

Output voltage	
High Level	1.1 V (typ.), terminate externally with 50 Ω to GND
Low Level	0.5 V (typ.), terminate externally with 50 Ω to GND
Rise / fall time (20% / 80 %)	55 ps (nom.)
Maximum data rate when controlled from FPGA A or B	16 Gb/s
Output impedance	50 Ω (nom.)
Connector	SMA

Reference Clock Input

Input frequency	100 MHz
Lock range	± 50 ppm (typ.)
Input level	632 mV_{pp} (0 dBm) to 3.1 V_{pp} (14 dBm) ± 1 dB (typ.)
Input impedance	50 Ω (nom.), AC coupled
Connector Type	SMA

Reference Clock Output

Reference Clock Source: Internal Reference Clock Oscillator	
Output frequency	100 MHz
Frequency accuracy	± 3 ppm initial accuracy (nom.), aging less than 20 ppm in 10 years (typ.)
Phase Noise	< -125 dBc/Hz at 10 kHz offset (meas.)
Output amplitude	850 mV ± 50 mV (typ.) Terminate externally with 50 Ω to GND
Reference Clock Source: External Reference Clock Input	
Output frequency	100 MHz
Frequency accuracy	Same as applied at Reference Clock Input
Phase Noise	determined by phase noise at Reference Clock Input
Output amplitude	850 mV ± 50 mV (typ.) Terminate externally with 50 Ω to GND
Source impedance	50 Ω (nom.), AC coupled
Connector type	SMA

General Purpose 'Control In/Out'

A parallel port with 5 digital input and 5 digital output signals is provided on the front panel.

Input assignment	Connected to 3 inputs per FPGA via switch matrix
Input range Low level High level	 0 V to +0.7 V (nom.) +1.6 V to +2.6 V (nom.)
Input impedance	Internal 1 kΩ (nom.) pull-down resistor, DC coupled
Input transition time	< 100 ns
Input hysteresis	10 mV (nom.)
Output assignment	Connected to 3 outputs per FPGA via switch matrix
Output range (TTL) Low Level (Output current -12 mA to 0 mA) High Level (Output current 0 mA to 12 mA)	 0 V to +0.4 V +2.4 V to +3.3 V
Connector Type	10-pin parallel coax connector Manufacturer Part Number: FCS-8 – 10 – 01. Connects with High Speed Coax Cable MPN: FCF-8-10-01. Manufacturer: Samtec.

FPGA Config Connector

An FPGA configuration connector is provided on the front panel to connect to an ILA (integrated logic analyzer) from Xilinx. In order to access an ILA within a customer partial region design, a Xilinx Vivado installation with Hardware Manager software and suitable cable drivers is required, inserting the male Micro USB B connector end of a suitable USB cable into the module, and the USB A connector end to the computer hosting the Xilinx software.

System Requirements

Operating System	Windows 8.1, 10 (64-bit)
Connection to AXIe hardware	PCIe or USB or Thunderbolt

General Characteristics [1]

Power consumption	280 W (nom.)
Operating temperature	0 °C to +40 °C
Operating humidity	5% to 80% relative humidity, non-condensing
Operating altitude	Up to 3000 m
Storage temperature	-40 °C to +70 °C
Stored states	User Configuration and factory default
Storage humidity	5% to 80% relative humidity, non-condensing
Operating random vibration [2]	Type tested at 5 to 500 Hz, 0.21 g RMS
Survival random vibration [2]	Type tested at 5 to 500 Hz, 2.09 g RMS
Power on state	Default
Interface to controlling PC	PCIe or USB (see AXIe specification)
Form factor	2-slot AXIe module
Dimensions (H x W x D)	60 mm x 322.5 mm x 281.5 mm
Weight	5 kg
Safety tested acc. to	IEC61010-1, ANSI/UL61010, CSA22.2 No. 61010-1 certified
EMC tested acc. to	IEC61326
Warm-up time	15 min
Calibration interval	n/a
Cooling requirements	Choose a location that provides at least 80 mm of clearance at rear, and at least 30 mm of clearance at each side.

1. Samples of this product have been tested in accordance with the Keysight Environmental Test Manual and verified to be robust against environmental stresses of storage, transportation, and end-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude, and power line conditions.
2. Test methods are according to IEC 60068-2-64 and levels are similar to MIL-PRF-28800F Class 3.

Definitions

Specification (spec.)

The warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0°C to 40°C and a 30-minute warm up period. Within ± 10°C after auto calibration. All specifications include measurement uncertainty and were created in compliance with ISO-17025 methods. Data published in this document are specifications (spec) only where specifically indicated.

Typical (typ.)

The characteristic performance, which 80% or more of manufactured instruments will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 23°C).

Nominal (nom.)

The mean or average characteristic performance, or the value of an attribute that is determined by design such as a connector type, physical dimension, or operating speed. This data is not warranted and is measured at room temperature (approximately 23°C).

Measured (meas.)

An attribute measured during development for purposes of communicating the expected performance. This data is not warranted and is measured at room temperature (approximately 23°C).

Accuracy

Represents the traceable accuracy of a specified parameter. Includes measurement error and timebase error, and calibration source uncertainty.

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