DATA SHEET

M8121A

12 GSa/s Streaming Arbitrary Waveform Generator

KEYSIGHT TECHNOLOGIES

M8121A at a glance

Key features

- 1 or 2 channel AWG module with
  - 14-bit resolution up to 8 GSa/s
  - 12-bit resolution up to 12 GSa/s
- Variable sample rate from 1 GSa/s to 8 or 12 GSa/s
- Analog bandwidth up to 5 GHz
- Spurious-free-dynamic range (SFDR) up to -90 dBc typical
- Harmonic distortion (HD) up to -72 dBc typical
- Internal broadband clock synthesizer with optional low-phase-noise clock input
- Optional real-time digital signal processing in Keysight Technologies, Inc. proprietary ASIC for digital up-conversion to IF[1]
- Form-factor: 2 U AXIe module, controlled via external PC or AXIe system controller

Optical data interface

- 2 x 160 Gb/s optical streaming interface
- Supports full rate, gapless streaming of samples into the M8121A from compatible storage, digital signal processing (DSP) or digitizer devices or custom hardware
- Synchronization input for deterministic latency e.g. from a digitizer input to M8121A output

Two output paths for different applications

- Direct DAC — optimized for best SFDR & HD
  - SFDR up to -90 dBc (typ), f_{out} = 100 MHz, measured DC to 2 GHz
  - Amplitude 350 mV_{pp} ... 700 mV_{pp}, offset –20 mV ... +20 mV
  - Differential output
- Optional DC coupled amplifier
  - Amplitude 500 mV_{pp} ... 1.0 V_{pp}; (over-programming down to 150 mV possible)
  - Output voltage window: –1.0 V … +3.3 V
  - Differential output

M8192A multi-channel synchronization module

- Phase coherent synchronization of up to six M8121A modules (= 12 channels)
- One trigger input can trigger up to six M8121A modules with deterministic latency
- Skew can be adjusted with 50 fs delay resolution between any two channels
- 1U AXIe module for high port density

[1] Requires option -DUC. Please contact Keysight for availability.

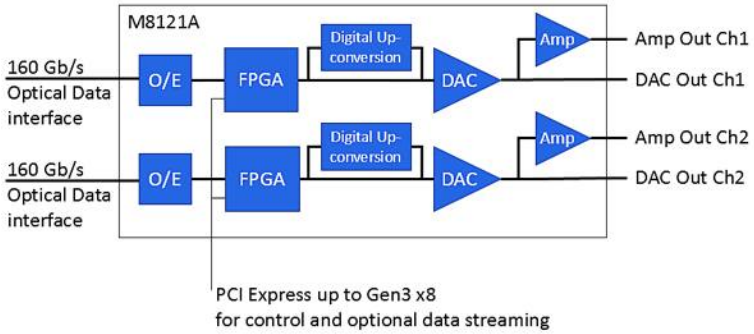
Scenario Generator with Infinite Playtime

Conventional AWGs have a certain amount of built-in waveform memory that allows the user to generate pre-calculated waveform segment(s) under the control of a sequencer.

But no matter how large the memory of an instrument is, it is a finite resource and eventually a loop will occur. Even the most complex sequencing engine does not eliminate this basic limitation.

The M8121A uses a different approach: Instead of a built-in memory, it offers a full rate optical data interface (ODI) to supply the samples to the DAC at up to 12 GSa/s via streaming, which enables infinitely long scenarios to be generated with up to approximately 5 GHz of modulation bandwidth.

The figure below shows an overview block diagram on the M8121A.



For modulation bandwidths up to approximately 250 MHz, the PCI Express interface to a host PC can be used to stream data into the AWG in a future release.[1]

[1] PCIe streaming is not available at initial release. Please contact Keysight for availability. .

High resolution, wide bandwidth and streaming combined

The M8121A not only offers a wide bandwidth streaming interface for infinite playtime, but with up to 14 bits of vertical resolution and up to -90 dBc of spur-free dynamic range (SFDR), the M8121A achieves best-in-class signal performance, which is a key requirement in many aerospace defense, wireless and high-end physics applications.

Flexibility

In addition to a “direct mode”, where DAC samples are transmitted over the streaming interface, it is possible to use the built-in “digital up-conversion” functionality.[1] In this mode, in-phase and quadrature (I/Q) baseband samples are supplied over the streaming interface. The signal is interpolated to the DAC sample rate, multiplied with the desired carrier frequency before it is sent to the DAC.

The benefits of this mode are:

- Lower data throughput over the streaming interface, which translates into longer playtime for a given amount of storage
- Flexibility of adjusting the waveform parameters (frequency, amplitude, phase) on the fly
- Extremely fine carrier frequency/phase resolution (down to nHz resp. 0.001 degrees)
- Absolutely no distortions like LO feed-through and images that occur with analog I/Q modulators

[1] Requires option DUC. Please contact Keysight for availability.

User Accessible FPGA[1]

For additional flexibility, the FPGAs in the M8121A can be made accessible to the user in a future release. This will allow users to develop their own proprietary functionality that will execute in real-time inside the instrument. Please check for availability.

Optical Data Interface

The AXIe Consortium (http://www.axiestandard.org/odispecifications.html) has standardized a high-speed optical data interface (ODI) for advanced instrumentation and embedded systems.

The M8121A has two ODI ports on the front panel, to receive data at up to 160 Gb/s per port. Each of the optical interfaces has sufficient throughput to support a 12 GSa/s signal with 12 bits of resolution (= 144 Gb/s), which corresponds to one M8121A channel at maximum sample rate.

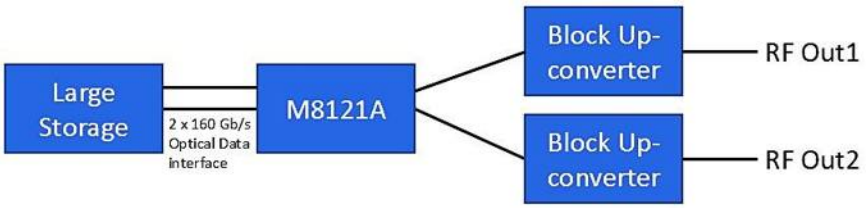
The optical data interface serves as a backbone between wideband AWGs, digitizers, digital signal processing modules, mass storage devices or custom hardware.

Due to the modular structure, different system configurations can be realized. A few examples are shown in the following paragraphs.

Applications

Wideband streaming

The M8121A together with a compatible mass storage device[2] offers the unique capability to generate non-repeating, wideband scenarios for minutes to hours – only limited by the capacity of the storage device. Combined with a compatible block up-converter[1], frequencies up to 44 GHz with modulation bandwidths up to 4 GHz can be covered.



Dynamic signal generation

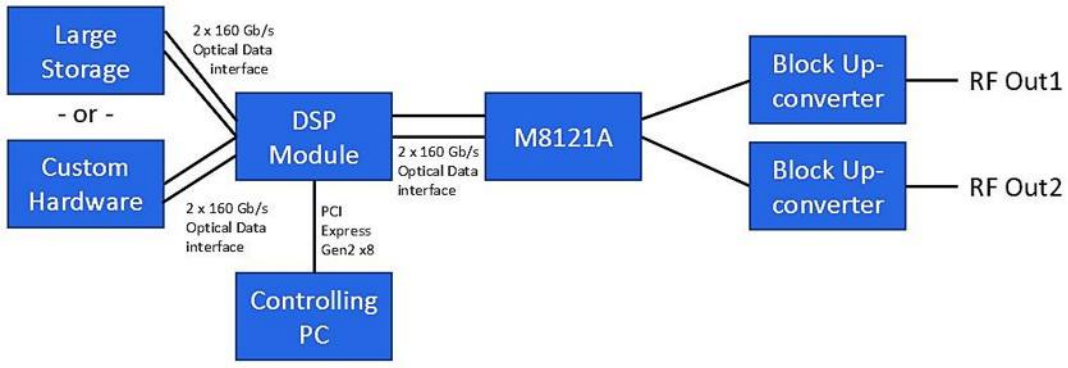
In many cases, the scenario that needs to be generated is not static, but it must be modified at runtime. In conjunction with a compatible digital signal processing module[1], the digital waveform that is transmitted to

[1] User accessible FPGA is not available at initial release. Please contact Keysight for availability.

[2] Please contact Keysight for further details.

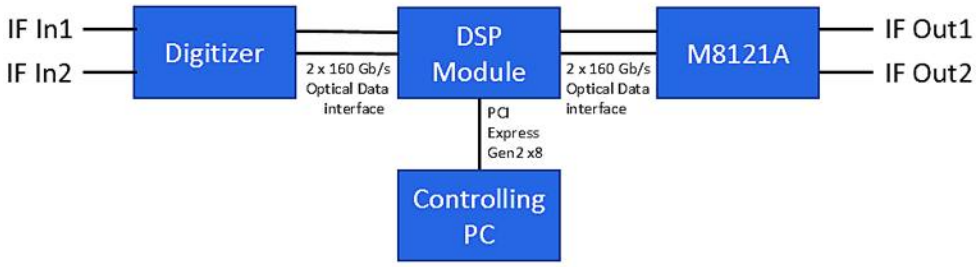
the AWG can be altered or even generated in real-time. Possible applications that can be realized include:

- Scenario playback with real-time modifications, such as adding noise or clutter
- Electromagnetic spectrum simulation
- Translation from pulse descriptor words into I/Q signals for radar simulations
- Adjusting the pulse delay in a radar target simulation



Record and playback

In combination with a compatible digitizer, it is possible to put together a very wideband record and playback system. Depending on the amount of processing required, one or more digital signal processing modules can be inserted in the path.



Front panel connections

Front Panel Connector	Description
ODI 1/2	Optical data interface connectors for channels 1 and 2
Flow Ctrl 1/2	Reserved for future use
Sample Mrk Out 1/2	Sample marker output, auxiliary digital output signal with sample clock resolution
Direct Out 1/2	Direct DAC output, normal and complement
Amp Out 1/2	Amplifier output, normal and complement
Sys Clk Out, Sys Clk In	Used in conjunction with M8192A sync module to share sample and vector clocks between modules[1]
Sample Clk In	External sample clock input
Sample Clk Out	Sample clock output
Ref Clk In/Out	Reference clock input/output
Vector Mrk 1/2	Vector marker output
Trigger In	Input for trigger signal to start DAC output[1]
Aux In	Reserved for future use
Sync In	Used in conjunction with M8131A digitizer for calibration purposes[1]
LPN Clk In, LPN Clk Out	Low phase noise sample clock input/output
FPGA config	Reserved for future use

[1] Support is available in software Version 2.0 and higher.

Product Structure

The M8121A has a modular product structure and requires and AXIe chassis and an embedded AXIe controller or external PC to be operational.

Description	Option	Software Upgradable	Comment
1 channel model	001	N/A	Must order either 001 or 002
2 channel model	002	Yes	
Operation up to 8 GSa/s	08G	N/A	Must order either 08G or 12G
Operation up to 12 GSa/s	12G	Yes	
Amplifier output path	AMP	Yes	Direct DAC output path can be used alternatively
Digital Up-conversion	DUC[1]	Yes	In DUC mode, sample rate is limited to 7.2 GSa/s
Low Phase Noise Mode	LPN	Yes	Requires external signal generator to supply low phase noise sample clock

Accessories

Description	Product #
Microwave phase matched balun, 6.5 GHz, max SMA jack	M8121A-801
Low pass filter, 2800 MHz, max SMA, VLF 2850+	M8121A-805
Low pass filter, 3900 MHZ max SMA, VLF 3800+	M8121A-806
Cable assembly coaxial–50 Ω, SMA to SMA, 457 mm length	M8121A-810
Cable assembly coaxial–50 Ω, SMA to SMA, 1220 mm length	M8121A-811
Additional Cable Assembly, semi-rigid, used in conjunction with M8121A-LPN	M8121A-812
Connector-RF, SMA termination, plug straight, 50 Ω, 12.4 GHz, 0.5 W	M8121A-820
Additional Optical Data Interface cable, 1m	M8121A-830
Additional Optical Data Interface cable, 3m	M8121A-831
Additional Optical Data Interface Loopback Jumper	M8121A-835

[1] Please contact Keysight for availability.

AXIe

The M8121A is a modular instrument packaged in the AXIe form factor. AXIe is a new open standard for high-performance, modular instrumentation, and incorporates the best features of other modular formats including VXIbus, LXI and PXI. Keysight offers a line of scalable chassis in this powerful format. Along with controller options, these AXIe chassis can form the basis of high-performance, AXIe-based test systems.

Two form factors are available: two-slot and five-slot chassis. These include an embedded AXIe system module that does not occupy a module slot. In addition, an AXIe controller is an entire PC that can control the AWG. This controller consumes one module slot in the chassis. The chassis can be used on the bench or in a rack, occupying only 4U of rack space.

Description	Product #
2-slot AXIe chassis	M9502A
5-slot AXIe chassis	M9505A
PCIe desktop card adapter Gen 2 x8	M9048A
x4 – x8 PCIe cable	Y1200B
x8 – x8 PCIe cable	Y1202A
Embedded AXIe controller	M9537A

Specifications

General characteristics

Sample Rate	
14-bit mode	1 GSa/s to 8 GSa/s
12-bit mode	1 GSa/s to 12 GSa/s
Effective output frequency (f_{max} is determined as $f_{Sa,max}/2.5$)	
14-bit mode	f_{max} = 3.2 GHz
12-bit mode	f_{max} = 4.8 GHz

Direct Out1/Direct Out2

Type of output	Single-ended[1] or differential, DC-coupled
Skew between normal and complement outputs	0 ps (nom)
Skew accuracy between normal and compl. outputs	± 5 ps (typ)
Impedance	50 Ω (nom)
Amplitude control	Specified into 50 Ω
Range, single-ended (DNRZ/NRZ Mode)[2]	350 mV_{pp} to 700 mV_{pp}
Resolution	30 µV (nom)
DC accuracy, (offset = 0 V, DNRZ/NRZ Mode)[2]	± (1.5% + 15 mV) (spec)
Offset	–20 mV to + 20 mV, single-ended into 50 Ω
Offset resolution	60 µV (nom)
DC offset accuracy	± 10 mV (spec) Common mode offset and differential offset is separately adjustable
Connector type	SMA

[1] Unused Output must be terminated with 50 Ω to GND. For best single ended performance, it is recommended to use differential signals in conjunction with a balun.

[2] Doublet mode does not allow DC signal generation.

NRZ/DNRZ mode

Bandwidth (3 dB)[1]	3.0 GHz (typ)
Bandwidth (5 dB)	5.0 GHz (typ)
Harmonic distortion[2,3] (7.2 GSa/s, 700 mV_{pp}, DNRZ)	-72 dBc (typ, f_{out} = 100 MHz)
	-68 dBc (typ), f_{out} = 10 MHz ... 500 MHz, measured DC to 3 GHz
	-60 dBc (typ), f_{out} = 500 MHz ... 1500 MHz, measured DC to 3 GHz
Harmonic distortion[3,4] (12 GSa/s, 700 mV_{pp}, DNRZ)	-54 dBc (typ), f_{out} = 100 MHz
	-50 dBc (typ), f_{out} = 10 MHz ... 2500 MHz, measured DC to 5 GHz
SFDR in 14 bit mode[2,3] (excluding harmonic distortion)	In Band Performance: -90 dBc (typ), f_{out} = 100 MHz, measured DC to 2 GHz -80 dBc (typ), f_{out} = 10 MHz…<500 MHz, measured DC to 500 MHz -76 dBc (typ), f_{out} = 500 MHz…<1 GHz, measured DC to 1 GHz -68 dBc (typ), f_{out} = 1 GHz…<2 GHz, measured DC to 2 GHz -62 dBc (typ), f_{out} = 2 GHz…3 GHz, measured DC to 3 GHz
	Adjacent Band Performance: -80 dBc (typ), f_{out} = 10 MHz…<500 MHz, measured DC to 1.5 GHz -73 dBc (typ), f_{out} = 500 MHz…<1 GHz, measured DC to 3 GHz -68 dBc (typ), f_{out} = 1 GHz…<2 GHz, measured DC to 3 GHz -62 dBc (typ), f_{out} = 2 GHz…3 GHz, measured DC to 3 GHz
SFDR in 12 bit mode[3,4] (excluding harmonic distortion)	In Band Performance: -90 dBc (typ), f_{out} = 100 MHz, measured DC to 2 GHz -80 dBc (typ), f_{out} = 10 MHz…<500 MHz, measured DC to 500 MHz -78 dBc (typ), f_{out} = 500 MHz…<1 GHz, measured DC to 1 GHz -73 dBc (typ), f_{out} = 1 GHz…<2 GHz, measured DC to 2 GHz -68 dBc (typ), f_{out} = 2 GHz…<3 GHz, measured DC to 3 GHz -60 dBc (typ), f_{out} = 3 GHz…5 GHz, measured DC to 5 GHz
	Adjacent Band Performance: -80 dBc (typ), f_{out} = 10 MHz…500 MHz, measured DC to 1.5 GHz -73 dBc (typ), f_{out} = 500 MHz…<1 GHz, measured DC to 3 GHz -68 dBc (typ), f_{out} = 1 GHz…<2 GHz, measured DC to 5 GHz -64 dBc (typ), f_{out} = 2 GHz…<3 GHz, measured DC to 5 GHz -60 dBc (typ), f_{out} = 3 GHz…5 GHz, measured DC to 5 GHz
Two-tone IMD[2]	-73 dBc (typ), f_{out1} = 499.5 MHz, f_{out2} = 500.5 MHz

[1] t_r bandwidth: BW = 0.25/t_r

[2] SCLK = 7.2 GSa/s, amplitude = 700 mV_{pp}, double NRZ mode, excluding f_{Sa}-2*f_{out}, f_{Sa}-3*f_{out}.

[3] Measured with a balun, such as the M8121A-801.

[4] SCLK = 12 GSa/s, amplitude = 700 mV_{pp}, double NRZ mode, excluding f_{Sa}-2*f_{out}, f_{Sa}-3*f_{out}.

Doublet mode[1]

Harmonics (14 bit, doublet mode, 8 GSa/s)[2]	fout = 5.4 GHz ... 6.5 GHz measured 5.4 GHz to 6.5 GHz, no harmonics in this range
Harmonics (12 bit, doublet mode, 12 GSa/s)[3]	fout = 8.1 GHz ... 9.9 GHz, measured 8.1 GHz to 9.9 GHz, no harmonics in this range
SFDR in 14 bit doublet mode[2] (excluding harmonic distortion)	–48 dBc (typ) fout = 5400 MHz ... 6500 MHz, measured 5.4 GHz to 6.5 GHz, single ended
SFDR in 12 bit doublet mode[3] (excluding harmonic distortion)	–44 dBc (typ) fout = 8100 MHz ... 9900 MHz, measured 8.1 GHz to 9.9 GHz, single ended

Amp Out1/Amp Out2[4]

Output type	Single ended[5] or differential, DC-coupled
Impedance	50 Ω (nom)
Amplitude	500 mV_{pp} to 1.0 V_{pp}, single-ended into 50 Ω (overprogramming down to 150 mV possible)
Amplitude resolution	300 µV (nom)
DC amplitude accuracy	± (2.5% + 10 mV) (nom)
Voltage window	-1.0 V to + 3.3 V[6], single-ended into 50 Ω
Offset resolution	600 uV (nom)
DC offset accuracy	± 2.5% ± 10 mV (typ) ± 4% of amplitude (typ)
Termination voltage window	–1.5 V to + 3.5 V [6]
Termination voltage resolution	300 µV (nom)[7]
Skew between normal and complement outputs	0 ps (nom)
Skew accuracy between normal and complement outputs	± 5 ps (typ)
Rise/fall time (20% to 80%)	< 60 ps (typ)[8]
Jitter	15 ps (typ)[8]
Connector type	SMA

[1] Doublet mode does not allow DC signal generation.

[2] SCLK = 8 GSa/s, amplitude = 700 mVp-p, double NRZ mode, excluding fSa – 2 * fout, fSa – 3 * fout.

[3] SCLK = 12 GSa/s, amplitude = 700 mVp-p, double NRZ mode, excluding fSa – 2 * fout, fSa – 3 * fout

[4] Option AMP required.

[5] Unused output must be terminated with 50 Ω to the termination voltage.

[6] Termination voltage window: offset +/- 1 V.

[7] Termination voltage = 0 V.

[8] PRBS 211 – 1, FSa = 12 GSa/s, data rate = 3 Gb/s, triggered on sample clock out

Marker Outputs

Number of marker outputs	Two markers per channel: sample marker and vector marker
Output type	Sample marker: single ended Vector marker: single ended
Output impedance	50 Ω (nom)
Level	
Voltage window	-0.5 V to 2.0 V
Amplitude	200 mVpp to 2.0 Vpp
Resolution	10 mV
Accuracy	± (10% + 25 mV) (typ)
Rise/fall time (20% to 80%)	150 ps (nom)
Connector type	SMA

Marker timing characteristics

Timing resolution, 12 or 14 bit direct mode	
Sample marker	1 sample clock cycle
Vector marker	64 sample clock cycles
Timing resolution, interpolated mode	
Sample marker	1 input IQ sample pair
Vector marker	32 input IQ sample pairs
Width, 12 bit direct mode	
Sample marker	49 sample clock cycles
Vector marker	User-defined in multiples of 64 sample clock cycles
Width, 14 bit direct mode	
Sample marker	40 sample clock cycles
Vector marker	User-defined in multiples of 64 sample clock cycles
Width, interpolated mode[1]	
Sample marker	Interpolation factor x3, x12, x24: 24 DAC output samples Interpolation factor x48: 48 DAC output samples
Vector marker	User-defined in multiples of (N*64) sample clock cycles, N = interpolation factor
Delay in 12 bit direct mode	
Sample marker to direct/AMP out	7.5 sample clock cycles – 1.75 ns (meas)
Vector marker to direct/AMP out	Channel 1: 3.7 ns (meas) Channel 2: 5 ns (meas)
Delay in 14 bit direct mode	
Sample marker to direct/AMP out	4.5 sample clock cycles – 1.75 ns (meas)
Vector marker to direct/AMP out	Channel 1: 3.7 ns (meas) Channel 2: 5 ns (meas)
Delay in Interpolated mode[1]	
Sample marker to direct/AMP out	3.5 sample clock cycles – 1.75 ns (meas)
Vector marker to direct/AMP out	TBD

[1] Requires option DUC. Please contact Keysight for availability.

Trigger Input

Input range	-5 V to +5 V
Threshold	
Range	-5 V to +5 V
Resolution	100 mV
Sensitivity	200 mV
Polarity	Selectable positive or negative
Drive	Selectable channel 1, channel 2, or both
Input Impedance	1 kΩ or 50 Ω (nom), DC coupled
Connector type	SMA

Trigger timing characteristics

Minimum pulse width	
Asynchronous	1.1 * vector clock period
Synchronous with Vector Clk Out	See set-up and hold timing
Setup time (Trigger In to rising edge of Vector Clk Out	1 ns (meas)
Hold time (Rising edge of Vector Clk Out to Trigger In)	-1 ns (meas)
Delay (Trigger In to Direct/DC Out)	4022.4 * sample clock period + 29.0 ns (meas)
Delay uncertainty	
Asynchronous	64 * sample clock period
Synchronous with Vector Clk Out	< sample clock period (nom)

Variable delay

In order to compensate for e.g. external cable length differences as well as the initial skew, channel 1 and channel 2 can be independently delayed with a very high timing resolution.

Setting the variable delay of channel 1 to 10 ps has following effect:

– Direct out1 (or amp out1, if selected) and sample marker out1 are delayed by 10 ps with respect to following signals: sample clock out, sync marker out1, sync marker out2, direct out2 (or amp out2, if selected).

Note: Modifying the variable delay of one channel always affects the delay of the analog output AND the sample marker of that channel. The delay is independently adjustable for channel 1 and 2.

Coarse delay	
Range	0 to 10 ns
Resolution	10 ps
Fine delay	
Range	
$f_{Sa} \geq 6.25$ GSa/s	0 to 30 ps
2.5 GSa/s ≤ fSa < 6.25 GSa/s	0 to 60 ps
$f_{Sa} < 2.5$ GSa/s	0 to 150 ps
Resolution	50 fs
Accuracy	
$f_{Sa} \geq 6.25$ GSa/s	± 10 ps (typ)
2.5 GSa/s ≤ fSa < 6.25 GSa/s	± 20 ps (typ)
$f_{Sa} < 2.5$ GSa/s	± 20 ps (typ)

Skew between channel 1 and channel 2

At a given sample rate, there can be some nominal amount of skew between channel 1 and channel 2. This can be calibrated out using the variable delay.

Skew repeatability[1]	2 ps (nom) without channel synchronization in between repeats[2] 20 ps (nom) with channel synchronization in between repeats[2]

[1] Variable delay is set to 0 ps, the channels are in coupled mode, and the same amplifier path for both channels is selected. Skew is measured on a real-time oscilloscope with averaging enabled.

[2] Channel synchronization is performed upon sample frequency or sample mode (i.e. 14- or 12-bit) change, and can introduce channel-to-channel skew variability.

Reference Clock Input

Input frequencies	Selectable 1 MHz to 200 MHz
Lock range	+/- 35 ppm (typ)
Frequency resolution	1 MHz
Input level	200 mV_{pp}, min (typ), 2 V_{pp}, max
Impedance	50 Ω, AC coupled (nom)
Connector Type	SMA

Reference Clock Output

Source: Internal backplane 100 MHz	
Frequency	100 MHz
Stability	+/- 20 ppm (typ) (see M9502A/M9505A data sheet)
Aging	+/- 1 ppm per year (nom)
Source: internal oven-controlled reference oscillator	
Frequency	100 MHz (nom)
Accuracy	+/- 0.2 ppm (nom)
Stability	+/- 0.6 ppm (typ)
Aging	+/- 0.3 ppm per year (typ)
Phase Noise	-95 dBc/Hz @ 10 Hz, -125 dBc/Hz @ 100 Hz offset (nom)
Source: External Ref. Clock In	
Frequency	100 MHz
Amplitude	1 V_{pp} into 50 Ω (nom)
Source impedance	50 Ω, AC coupled (nom)
Connector Type	SMA

Vector clock output

Frequency	
14 or 12 bit direct mode	Sample clock divided by 64
Interpolated mode[1]	Sample clock divided by 32
Output amplitude	1 V_{pp} into 50 Ω (nom)
Impedance	50 Ω, AC coupled (nom)
Connector Type	SMA

[1] Requires option DUC. Please contact Keysight for availability.

Sample clock

There are three selectable sources for the sample clock:

- Internal synthesizer
- Sample clock input
- Low phase-noise clock input

Internal synthesizer clock

Frequency	1 GHz to 12 GHz
Accuracy	+/- 20 ppm (typ)
Frequency resolution	15 digits, e.g. 10 µHz at 1 GHz
Phase noise	f_{Sa} = 1 GHz < –110 dBc/Hz (typ) at 10 kHz offset, f_{out} = 125 MHz[1] f_{Sa} = 8 GHz < –105 dBc/Hz (typ) at 10 kHz offset, f_{out} = 1.0 GHz[1] f_{Sa} = 12 GHz < –105 dBc/Hz (typ) at 10 kHz offset, f_{out} = 1.5 GHz[1]

Sample clock input

Frequency range	1 GHz to 12 GHz
Input power range	+0 dBm to +7 dBm
Damage level	+8 dBm
Impedance	50 Ω, AC coupled (nom)
Connector Type	SMA

Low phase noise clock input[2]

The fine delay feature is disabled when using LPN clock. The frequency of the external low phase noise clock must be set in the External Sample Frequency box on the clock panel.

All other features of the instrument function the same as for standard operation.

Frequency range	1 GHz to 12 GHz
Input power range	+4 dBm to +7 dBm
Damage level	+10 dBm
Impedance	50 Ω, AC coupled (nom)
Connector Type	SMA

[1] Measured at Direct Out.

[2] Only with option LPN.

Sample Clock Output

Source	Internal synthesizer or sample clock input, whichever is selected
Frequency Range	1 GHz to 12 GHz
Output amplitude	300 mV_{pp} (nom), fixed
Input impedance	50 Ω, AC coupled (nom)
Transition time (20% to 80%)	30 ps (typ)
Connector Type	SMA

Optical Data Interface

The Optical Data Interface (ODI) is a high-speed interface standard for advanced instrumentation from the AXIe Consortium. Documentation of the ODI specification can be found at www.axiestandard.org/odispecifications.html.

ODI Physical Interface characteristics

Specification	ODI-1: Physical Layer Specification, Revision 3.0
Number of ODI ports	2 (one for each AWG channel)
Connector	MPO style, 2 rows of 12 fiber positions
Lane rate	14.1 Gbit/s
Interlaken Burst Max	2048 byte
Flow control	Selectable: None or in-band
Port Directionality	Consumer only (Bi-directional for self test purposes)
Port Aggregation	Not applicable
Interlaken Channels	1 channel (Ch 0)
Streaming Data Rate	20 GByte/s

ODI Data Format capability

Specification	ODI-2: Transport Layer, Revision 3.0, ODI-2.1: High Speed Data Formats, Revision 3.0
Packet Types supported	NO_HEADER
Context packets	Not used
Control packets	Not used
Timestamp support	None
Trailer bit support	None
Data Format Class IDs supported	See table below
Signal Data Packet Size	Selectable: None or in-band

Supported Data Format and Class ID Table

Item Packing Field Width	Data Item (signed)	Event bits	Real or IQ	Chan-nels	Notes
16	14 bit	2	Real	1	14 bit samples (direct mode), 2 marker bits
16	12 bit	4	Real	1	12 bit samples (direct mode), 2 marker bits, 2 don't care
12	12 bit	0	Real	1	12 bit samples, packed (link-efficient), no marker bits
16	15 bit	1	IQ	1	15 bit I/Q samples, 1 marker bit each for I and Q[1]

Digital up-conversion[1]

Sample rate	1 GSa/s to 7.2 GSa/s	
Carrier frequency		
Range	0 Hz to 12 GHz (observe frequency response and sin x/x roll-off)	
Resolution	Sample Clock / 2^{72}	
Amplitude range	0 to 100%	
Amplitude resolution	20,000 steps	
Vertical resolution IQ	15 bit samples for I and Q	
Vertical resolution DAC	14 bit, independent of 12 bit mode and 14 bit mode	
Interpolation factors	x3, x12, x24, x48	
SFDR and harmonics	See specs in 14 bit mode	
Mode dependent modulation bandwidth	Max. I/Q sample rate	Max. modulation bandwidth
Interpolation factor x3	2400 MSa/s	1920 MHz
Interpolation factor x12	600 MSa/s	480 MHz
Interpolation factor x24	300 MSa/s	240 MHz
Interpolation factor x48	150 MSa/s	120 MHz
Modulation BW ripple	0.8 x F_{Sa}, where F_{Sa} is the input I/Q sample rate, max 1 dB	

[1] Requires option DUC. Please contact Keysight for availability.

System and Software

Operating system	Windows 7, 8.1, 10; all 64-bit
Connection to AXIe hardware	PCIe
Application software	A graphical user interface (GUI or soft front panel) is offered to control all functionality.
Automation	Remote control via SCPI

General Characteristics

Power consumption	190 W (nom., 12 GSa/s operation)
Operating temperature	0 °C to +40 °C
Operating humidity	5% to 80% relative humidity, non-condensing
Operating altitude	Up to 2000 m
Storage temperature	-40 °C to +70 °C
Stored states	User Configuration and factory default
Power on state	Default
Interface to controlling PC	PCIe (see AXIe specification)
Form factor	2-slot AXIe module
Dimensions (H x W x D)	60 mm x 322.5 mm x 281.5 mm
Weight	6 kg
Safety designed to	IEC61010-1, UL61010, CSA22.2 61010.1 certified
EMC tested to	IEC61326
Warm-up time	30 min
Calibration interval	2 years recommended
Warranty	1 year standard
Cooling requirements	Do NOT block vents and fan exhaust. To ensure adequate cooling and ventilation, leave a gap of at least 50mm (2") around vent holes on both sides of the chassis.

Definitions

Specification (spec.)

The warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0°C to 40°C and a 30-minute warm up period. Within +/- 10°C after auto calibration. All specifications include measurement uncertainty and were created in compliance with ISO-17025 methods. Data published in this document are specifications (spec) only where specifically indicated.

Typical (typ.)

The characteristic performance, which 80% or more of manufactured instruments will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 23°C).

Nominal (nom.)

The mean or average characteristic performance, or the value of an attribute that is determined by design such as a connector type, physical dimension, or operating speed. This data is not warranted and is measured at room temperature (approximately 23°C).

Measured (meas.)

An attribute measured during development for purposes of communicating the expected performance. This data is not warranted and is measured at room temperature (approximately 23°C).

Accuracy

Represents the traceable accuracy of a specified parameter. Includes measurement error and timebase error, and calibration source uncertainty.

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