DATA SHEET

M3100A PXIe Digitizers With Optional Real-Time Sequencing and FPGA Programming

100 MSa/s, 14 Bits, 4/8 Channels

Improve Your Measurement Fidelity, Signal Integrity and Measurement Throughput

The M3102A are high-performance, high-bandwidth digitizers with an advanced data acquisition system (DAQ). Performance meets simplicity thanks to easy-to-use programming libraries, real-time sequencing technology (HVI Hard Virtual Instrumentation), and graphical FPGA programming technology.

Applications

- General purpose digitizer
- Hardware-in-the-loop (HIL) / Automated test equipment (ATE)
- R&D/scientific research equipment
- Aerospace & defense (A/D)

Features

100 MSa/s simultaneous sampling, 14 bits, 4/8 channels, 100 MHz BW [1]

Advanced data acquisition system (DAQ)

- Flexible triggering (HW trigger, HVI trigger, SW trigger)
- Programmable cycles and data bursts to avoid PC saturation

Optional HW programming for high-performance applications

- Real-time sequencing (HVI technology)
- FPGA programming
  - Xilinx Kintex-7, 325T or 410T FPGA

Up to 2 GB of onboard RAM (~ 1 Gsamples)

Mechanical/interface

- 1 slot 3U (PXIe)
- PCIe Gen 1
- Independent DMA channels for fast and efficient data transfer

1. 100 MHz refer to the Front End bandwidth. This digitizer can operate in 1st and 2nd Nyquist zones (using undersampling technique), but its real-time BW is limited by Nyquist to some 50 MHz. As an example for a band-limited signal of 70 MHz with a 10 MHz signal bandwidth, the aliased component will appear between 25 to 35 MHz (30 ± 5 MHz).

KEYSIGHT TECHNOLOGIES

Programming Technology and Software Tools

Software programming

- Easy-to-use native programming libraries for most common languages: C, C++, Visual Studio, LabVIEW, MATLAB, Python

Hardware programming (optional)

- Real-time sequencing (Hard Virtual Instrumentation or HVI technology)
  - Graphical flowchart-style M3601A design environment (-HV1 option required on HW)
  - Ultra-fast, fully-parallelized hard real-time execution
  - Ultra-fast, time-deterministic decision-making
  - Off-the-shelf inter-module synchronization & data exchange
- FPGA programming
  - FPGA design environment and BSP support
  - Supports VHDL, Verilog and Xilinx projects, and Xilinx IP Catalog
  - Ultra-fast, one-click compiling and on-the-fly programming

SD1 2.x and SD1 3.x differences

Keysight SD1 2.x software has been upgraded to 3.x. The key differences are listed in the table below. For more detail on SD1 3.x software, refer to the Start Up Guide M3xxx-90002.

WARNING **The 3.X version of software does not support programs using the M3601A or the M3602A applications. You will have to transition to KS2201A and KF9000A respectively.**

SD1 software features	Legacy (SD1 2.1.x)	New (SD1 3.x)
Software		
Design Environment	M3601A HVI design environment (ProcessFlow)	KS2201A PathWave Test Sync Executive (HVI2 technology)
	M3602A FPGA design environment (FPGAFlow)	KF9000A PathWave FPGA Programming Environment (commonly known as PathWave FPGA)
HVI Technology	Graphical M3601A for HV1	KS2201A PathWave Test Sync Executive (HVI2 Core API through a separate HVI installer)
	HVI-C API (through SD1 installer)	
FPGA Programming	Graphical M3602A	KF9000A PathWave FPGA (BSP installer for each supported module is required)
	PathWave FPGA (BSP for SD1 2.1.x only)	
Soft Front Panel (SFP)	Available	Available
Programming Interface	Python [1], C++, C#, LabVIEW, MATLAB	Python [1], C, C++, C#, LabVIEW, MATLAB
Supported Operating System	Windows 10 (32 / 64 bit)	Windows 10 (64 bit)

SD1 software features	Legacy (SD1 2.1.x)	New (SD1 3.x)
Hardware modules		
M3202A (AWG 1G)	FW version < 4.0 (CH4) (CLF) (K16, K32, K41)	FW version > =4.0 (CH4) (CLF / CLV**) (K16, K32, K41)
	BSP available (K32, K41)	BSP available (K32, K41)
M3201A (AWG 500)	FW version < 4.0 (CH4) (CLF) (K16, K32, K41)	FW version > =4.0 (CH4) (CLF / CLV**) (K16, K32, K41)
	BSP available (K32, K41)	BSP available (K32, K41)
M3102A (DIG 500)	FW version < 2.0 (CH4) (CLF) (K16, K32, K41)	FW version > =2.0 (CH4) (CLF) (K16, K32, K41)
	BSP available (K32, K41)	BSP available (K32, K41)
M3100A (DIG 100)	FW version < 2.0 (CH4 or CH8) (CLF) (K16, K32, K41)	FW version > =2.0 (CH4 or CH8) (CLF) (K32, K41)
	BSP available (K32, K41)	BSP available (K32, K41)
M3302A (COMBO 500 500)	FW version < 4.0 (CH2 AWG - CH2 DIG) (CLF) (K32*, K41)	FW version > =4.0 (CH2 AWG - CH2 DIG) (CLF) (K41)
	BSP available (K32*, K41)	BSP available (K41)
M3300A (COMBO 500 100)	FW version < 4.0 (CH2 AWG - CH4 DIG or CH4 AWG - CH8 DIG) (CLF) (K32*, K41)	FW version > =4.0 (CH2 AWG - CH4 DIG or CH4 AWG - CH8 DIG) (CLF) (K41)
	BSP available (K32*)	BSP available (K41)
No programming		
Easily configurable SD1 SFP (software front panel) interface for each connected module		

1. HVI programming is supported with Python version 3.7 only.
* This Hardware Option cannot be procured. Contact Keysight Support for more information.
** Only Default Clock Speed is supported. Variable Clock is NOT Supported.

PXIe Arbitrary Waveform Generators, Digitizers and Combination Modules

Product	Type	Outputs (AWGs)				Inputs (Digitizers)			
		Speed (MSa/s)	Bits	Ch	BW (MHz)	Speed (MSa/s)	Bits	Ch	BW (MHz)
M3202A	AWG	1000	14	4	DC-400				
M3201A	AWG	500	16	4	DC-200				
M3102A	Digitizer					500	14	4	DC-200
M3100A	Digitizer					100	14	4/8	DC-100
M3302A	Combo	500	16	2	DC-200	500	14	2	DC-200
M3300A	Combo	500	16	2/4	DC-200	100	14	4/8	DC-100

Functional Block Diagram

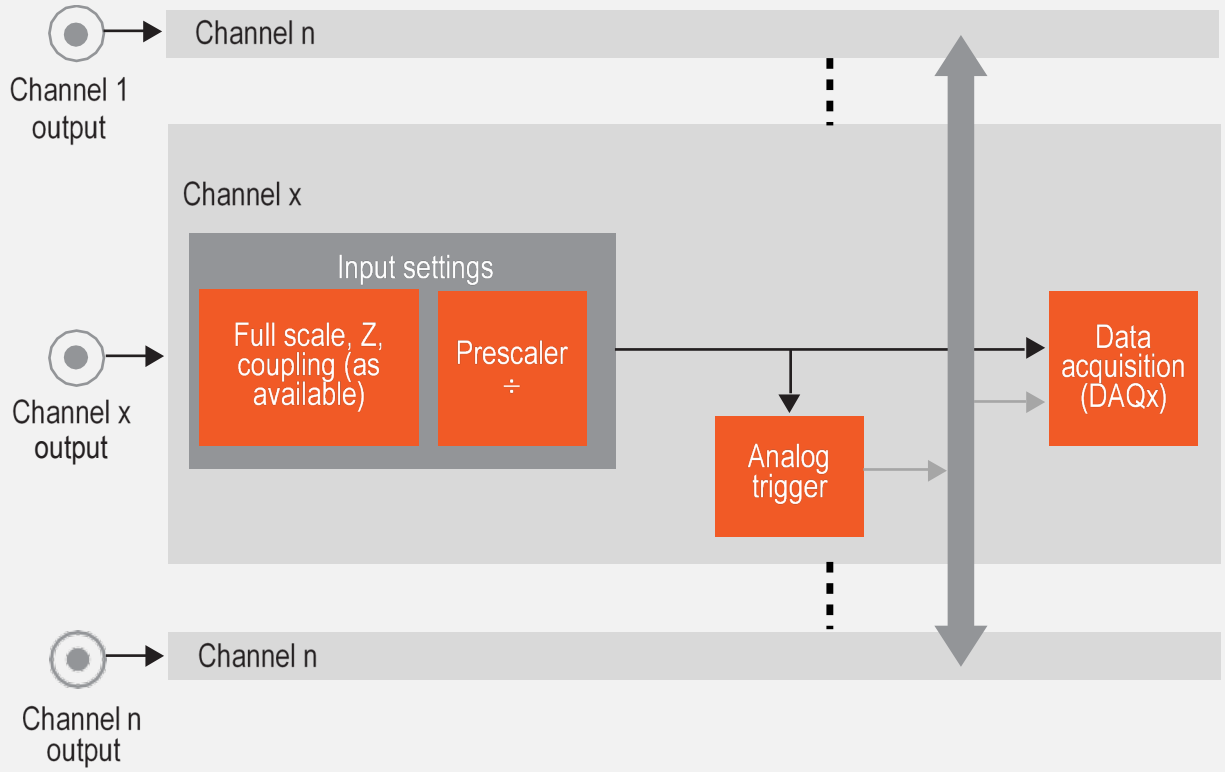


Figure 1. M3100A input functional block diagram, all channels have identical input structure

Ordering Information [1]

Product	Description
M3100A	PXIe digitizer: 100 MSa/s, 14 Bits
Options	**Description**
M3100A-CH4 / -CH8	Four channels [2] / eight channels
M3100A-CLF	Fixed sampling clock, low jitter [2]
M3100A-M01 / -M12 / -M20	Memory 16 MB, 8 MSamples [2] / 128 MB, 60 MSamples / 2 GB, 1 GSamples
HW Programming Options	**Description**
M3100A-HVI	Enables HVI programming, requires the -HV1 option and the HVI software license (KS2201A)
M3100A-FP1	Enables FPGA programming, requires -K41 option and an FPGA design environment license (KF9000A)
M3100A-K32 / K41	FPGA, Xilinx 7K325T / 7K410T, required for -FP1 option only (needs memory option -M20)
Related Software [3]	**Description**
M3601A	HVI design environment
M3602A	FPGA design environment
KS2201A	PathWave Test Sync Executive
KF9000A	PathWave FPGA

1. All options must be selected at time of purchase and are not upgradable
2. These options represent the standard configuration
3. M3601A / M3602A are supported with SD1 2.x software only, whereas KS2201A / KF9000A are supported with SD1 3.x software only.

Technical Specifications and Characteristics

General characteristics

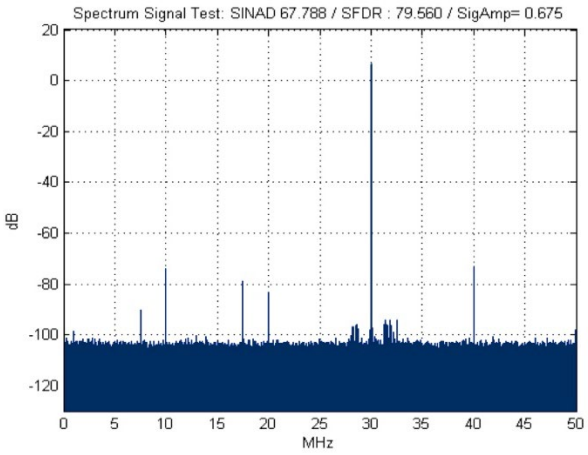
Parameter	M3100A-CH4			M3100A-CH8			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
Inputs and outputs								
Channels		4			8		Out	
Reference clock [1]		1			1		Out	
Reference clock [2]		1			1		In	
Triggers/markers [1, 3]		1			1		In/out	Reconfigurable
Triggers/markers [2, 3]		8			8		In/out	Reconfigurable
Input channels overview								
Sampling rate		100			100		MSa/s	
Voltage resolution		14			14		Bits	
Input frequency	DC		100	DC		100	MHz	
Real-time BW		50			50		MHz	
Time skew		< 50			<50		ps	Between channels
Built-in functionalities								
Sampling rate		4			8			1 per channel
Voltage resolution		4			8			1 per channel
Input frequency		4			8			1 per channel
Onboard memory								
RAM memory	16		2048	16		2048	MBytes	

1. At front panel
2. At backplane
3. Markers available from SD1 software version 3.0 onwards.

I/O specifications

Analog input characteristics	
Number of channels	CH4 or CH8
Sampling rate	100 MSa/s option CLF
Configurable inputs: Impedance	50Ω or 1 MΩ (Hi-Z)
Configurable inputs: Coupling	AC or DC
Input voltage range (50Ω)	400 mVpp to 6Vpp (continue: variable attenuator at input)
Input voltage range (Hi-Z)	200 mVpp to 20Vpp (continue: variable attenuator at input)
Bandwidth limit filters	100 MHz
Effective number of bits (ENOB) [1]	10.8 bits @30MHz (typical)
Noise floor	−142 dBm/Hz @30 MHz (typical)
SINAD	67 dB @30 MHz (typical)
Spurious free dynamic range (SFDR) + Total Harmonic Distortion [1]	79 dBc (typical)

1. Measured at -1 DBFS input signal with 1.5 Vpp 50Ω



Parameter	M3100A			Units	Comments
	Min	Typ	Max		
Reference clock output					
Frequency		10 or 100		MHz	Generated from the internal clock, user selectable
Voltage		800		mV_{pp}	On a 50 Ω load
Power		2		dBm	On a 50 Ω load
Source impedance		50		Ω	AC coupled
External I/O trigger/marker					
V_{IH}	2		5	V	
V_{IL}	0		0.8	V	
V_{OH}	2.4		3.3	V	On a high Z load
V_{OL}	0		0.5	V	On a high Z load
Input impedance		10		K Ω	
Source impedance		TTL		–	
Speed			500	Mbps	

Data acquisition blocks (DAQs) specifications

Parameter	M3100A-CH4			M3100A-CH8			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
General specifications								
DAQs		4			8			1 per channel
Aggregated speed			400			800	MSa/s	For all onboard DAQs combined
Acquisition burst multiple		5			5		Samples	Burst length must be a multiple of this value
Acquisition RAM capacity	16		957M	16		957M	Samples	Maximum depends on onboard RAM and the number of samples per cycle must be even number
Acquisition RAM capacity effic.		93.5			93.5		%	Efficient = waveform size / waveform size in RAM
Trigger		Select			Select			Hardware trigger (analog channels, input trigger, backplane triggers), SW/HVI trigger
DAQ specifications								
Speed			100			100	MSa/s	Per DAQ
Resolution		14			14		Bits	

Clock system specifications

Parameter	M3100A-CH4			M3100A-CH8			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
General specifications								
Clock frequency		100			100		MHz	

System Specifications

Environmental specifications (PXI Express)

Parameter	M3100A-CH4			M3100A-CH8			Units	Comments
	Min	Typ	Max	Min	Typ	Max		
System bus								
Slots		1			1		Slot	PXI Express (CompactPCI Express compatible)
PCI Express type		Gen 1			Gen 1		–	Chassis dependent
PCI Express link	1		4	1		4	Lanes	Automatic lane negotiation, chassis dependent
PCI Express speed	400		1600	400		1600	MBytes/s	Depends on # of lanes, chassis, congestion, and more
Power dissipation								
3.3V PXIe power supply		1.5			1.5		A	~ 5 W
12V PXIe power supply		2			2		A	~ 24 W

Environmental specifications (PXI Express)

Environmental [1]		
Temperature range	Operating Non-operating	0 to +55°C (10,000 feet) -40 to +70 °C (up to 15,000 feet)
Max operative altitude		3000 m (10,000 feet)
Operating Humidity range (%RH)		10 to 95% at 40°C
Non-operating Humidity range (%RH)		5 to 95%
EMC		Complies with European EMC Directive – IEC/EN 61326-1 – CISPR Pub 11 Group 1, class A This ISM device is in compliance with Canadian ICES-001 Cet appareil ISM est conforme à la norme NMB-001 du Canada This ISM device is in compliance with Australian and New Zealand RCM This ISM device is in compliance with South Korea EMC KCC

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

www.keysight.com/find/m3100a

Learn more at: www.keysight.com

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at: www.keysight.com/find/contactus

KEYSIGHT TECHNOLOGIES