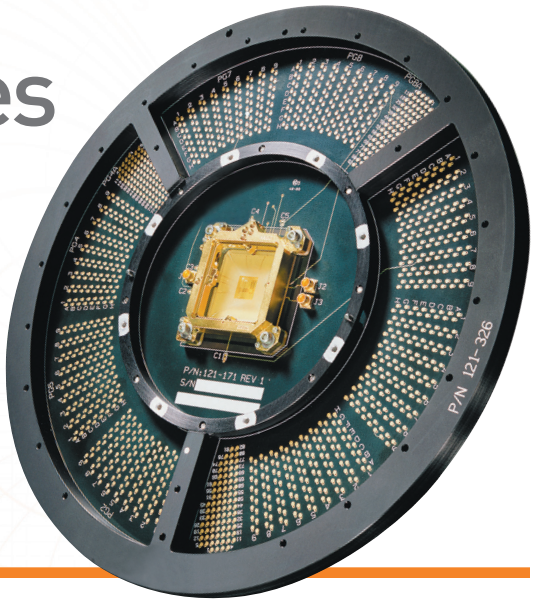
SiP/SoC Series

High-performance SiP/SoC Pyramid Probe® card



DATA SHEET

Cascade Microtech's high-performance SiP/SoC Pyramid Probe cards reduce your cost of ownership through enhanced throughput, reduced maintenance and increased yields — enabled by large multi-DUT probe surfaces, permanent probe alignment, superior electrical performance and long life. Designed for both bond-pad and flip-chip bump applications, the SiP/SoC Pyramid Probe allows at-speed testing of large-scale ICs at die sort. Low inductance power, ground contacts and controlled impedance signal lines provide electrical performance exceeding most IC packages. At-speed die sort reduces scrap and allows shipment of Known-Good Die (KGD).

FEATURES / BENEFITS

Superior signal performance	High-bandwidth RF Microstrip transmission lines to probe tips guarantee performance and ensure low signal loss. Consistent low contact resistance and low-inductance probe tips ensure accurate and repeatable high-speed digital and analog measurements. Patented ground and power planes with bypass capacitors provide resonance-free stable power supplies directly to the multi-DUTs.
Mechanical robustness	MicroScrub® technology provides consistent low contact resistance and inductance on a variety of pad materials and flip-chip bumps. High-density photolithographically-placed contact probe tips are stable over lifetime of product. Low maintenance and permanent probe tip placement improve test cell uptime, reducing the cost of ownership compared to other probing technologies.
Versatile and cost-effective	Lower maintenance overhead with less cleaning and no need for probe tip alignment.
Advanced membrane technology	Cascade Microtech's industry-leading Pyramid Plus™ manufacturing process delivers higher performance, plus unique features that lower your cost of test.

CascadeMicrotech®

MECHANICAL

Minimum pitch	50 µm
Staggered pitch	36 µm/72 µm
Dimensional stability for lifetime	10 µm for single temperature
Probe tip size Al, Cu (nominal)	12 µm
Probe tip size Low K/PoAA (nominal)	18 µm
Probe tip size Au, solder balls (nominal)	25 µm
Probe tip material	Non-oxidizing nickel alloy
Temperature range	-50°C to 125°C
Pad and bump materials	Al, Cu, Au, all types of solder balls
Spring rate	1.67 g/mil
Edge sense	Optional

ELECTRICAL

Leakage	1 nA/V
Contact resistance	0.1 to 0.2 Ω (Al pads), 0.005 to 0.010 Ω (Au pads)
Maximum current / tip	1 A (Au pads), 200 mA (Al pads, Cu pads and solder balls)
Maximum power 50 Ω microstrip	+33 dBm CW, +36 dBm pulsed
Maximum power 50 Ω Co-Planar Waveguide (CPW)	+33 dBm CW, +39 dBm pulsed

POWER SUPPLY PERFORMANCE

Power trace impedance	10 Ω
Inductance to first capacitor	0.2 nH
Maximum current std power trace	1 A
Maximum current per power supply	10 A

SIGNAL TRACE PERFORMANCE

Standard

Signal line impedance	50 Ω nominal
Ground inductance (typical)	0.04 nH
Return loss (S_{11}) to coax	>10 dB @ 20 GHz
Input reflection	±80 mrho @ 50 Ω

Optional

Range of trace impedances	2 Ω to 120 Ω ±20%
Differential impedance	50 Ω, 100 Ω and 200 Ω

SIGNAL TRACE LENGTH MATCHING

Typical signal	No match
Optimized signal (custom layout)	±1.5 ps (3 ps window)

SERIES PATH RESISTANCE (SPR)

	P100	P300	P400	P500	P800
DC resistance	1 Ω	1 Ω	1.6 Ω	2.5 Ω	2.5 Ω
Microstrip	1.2 Ω	1.2 Ω	2 Ω	3 Ω	3 Ω
CPW	0.8 Ω	0.8 Ω	1 Ω	1.2 Ω	1.2 Ω

COMPONENTS ATTACHED TO MEMBRANE

Package type	SMT
Sizes	0201, 0402 (preferred), 0603, 0805

COMPONENTS DEFINED WITHIN MEMBRANE

Inductors	0.3 nH to1 nH (±0.3 nH)
Inductors	1 nH to 10 nH (±30 %)
Trimmed inductors	0.3 nH to 10 nH (±0.1 nH)
Capacitors	20 fF to 2 pF (±20 %)

PYRAMID CORE OPTIONS

	P100	P300	P400	P500	P800
I/O capacity	108	264	408	520	804
XY area (mm)	4.1 x 4.1	4.1 x 4.1	9.6 x 9.6	24 x 24	38 x 11
Components on core	32	32	40	100	120

RF-CLASS BANDWIDTH AND RISETIME PERFORMANCE

TRANSMISSION LINE			FRAME CORE BANDWIDTH AND RISE TIME				
Membrane	PCB	Connector	P100	P300	P400	P500	P800
Microstrip	Microstrip	Pogo pad	2 GHz 200 ps	2 GHz 200 ps	2 GHz 200 ps	2 GHz 200 ps	2 GHz 200 ps
Microstrip	Microstrip	PCB coaxial	7 GHz 50 ps	7 GHz 50 ps	7 GHz 50 ps	7 GHz 50 ps	7 GHz 50 ps
Microstrip	Coax	K or V	20 GHz 22 ps	20 GHz 22 ps	20 GHz 22 ps	15 GHz 25 ps	20 GHz 22 ps
CPW	Coax	K or V	20 GHz 15 ps	20 GHz 15 ps	20 GHz 17 ps	20 GHz 22 ps	20 GHz 17 ps

PYRAMID CORE NAME CORRELATION

Previous frame core name	RFC	SRF	MSI	LSI	VLSR
Current frame core name	P100	P300	P400	P500	P800

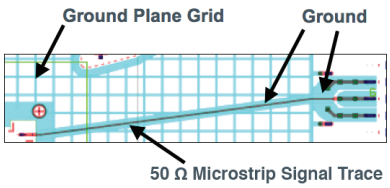
50 Ω SIGNAL TRACE OPTIONS

Microstrip

Standard option

Higher routing density/Smaller trace width

Best choice for isolation

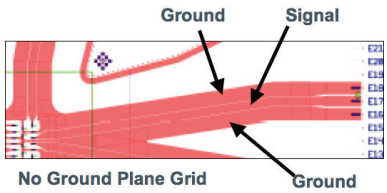


Coplanar Waveguide (CPW)

Optional

Lower routing density/Wider trace width (GSG)

Higher power/Lower path resistance



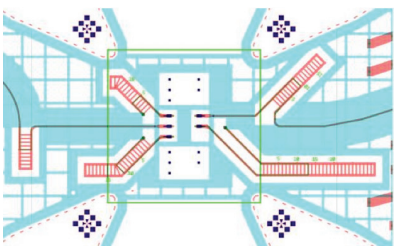
EMULATING LEAD INDUCTANCE

Some circuits require proper inductive loading

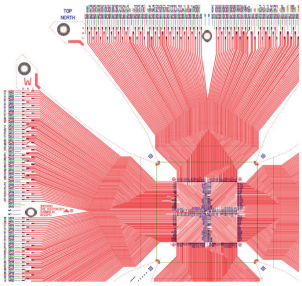
Effects cannot be calibrated out easily

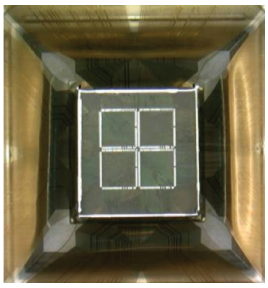
Embed inductance on all interface pins into probe card

Do not calibrate past lead inductance structures



MULTI-DUT TESTING (CELL PHONE PROCESSOR)





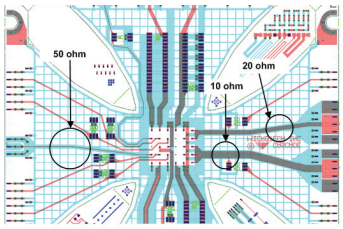
IMPEDANCE MATCHING

Not all devices operate at 50 Ω

Matching to real impedance is needed for many tests

Incorporate into probe card

Many techniques:
- Lumped element
- Quarter wave transmission line
- Combination



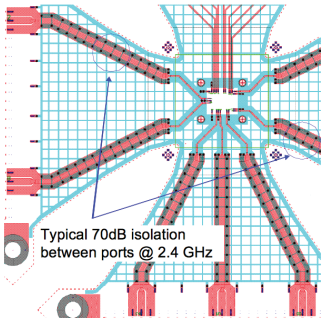
ISOLATION/CROSSTALK

Port-to-port coupling must be less than the DUT

Contain the fields within closed structures when possible

Separate ports as best as possible

Consider pad layout for isolation and test setup validation



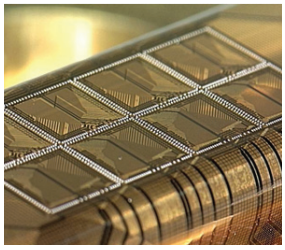
Example: Multi-position RF switch

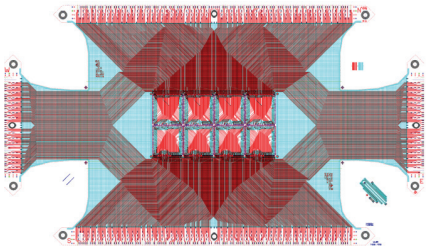
CORE LAYOUT 2x4 ARRAY

12 x 24 mm area

55 µm pad size

800 signals





PyramidSiPSoC-DS-0212

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