P5960
High-Density D-MAX Probe
for TLA6400 Series Logic Analyzers

Instruction Manual

Warning

The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

www.tektronix.com

077-0637-01

Tektronix

Contacting Tektronix

Tektronix, Inc.
14150 SW Karl Braun Drive
P.O. Box 500
Beaverton, OR 97077
USA

For product information, sales, service, and technical support:

- In North America, call 1-800-833-9200.
- Worldwide, visit www.tektronix.com to find contacts in your area.

Warranty

Tektronix warrants that this product will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If any such product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product. Parts, modules and replacement products used by Tektronix for warranty work may be new or reconditioned to like new performance. All replaced parts, modules and products become the property of Tektronix.

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General safety summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of a larger system. Read the safety sections of the other component manuals for warnings and cautions related to operating the system.

To avoid fire or personal injury

Connect and disconnect properly. Connect the probe output to the measurement instrument before connecting the probe to the circuit under test. Connect the probe reference lead to the circuit under test before connecting the probe input. Disconnect the probe input and the probe reference lead from the circuit under test before disconnecting the probe from the measurement instrument.

Ground the product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe all terminal ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

The inputs are not rated for connection to mains or Category II, III, or IV circuits.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Power disconnect. The power cord disconnects the product from the power source. Do not block the power cord; it must remain accessible to the user at all times.

Do not operate without covers. Do not operate this product with covers or panels removed.

Do not operate with suspected failures. If you suspect that there is damage to this product, have it inspected by qualified service personnel.

Avoid exposed circuitry. Do not touch exposed connections and components when power is present.

Use proper fuse. Use only the fuse type and rating specified for this product.

Do not operate in wet/damp conditions.

Do not operate in an explosive atmosphere.

Keep product surfaces clean and dry.

Provide proper ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Terms in this manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Symbols and terms on the product

These terms may appear on the product:

- DANGER indicates an injury hazard immediately accessible as you read the marking.
- WARNING indicates an injury hazard not immediately accessible as you read the marking.
- CAUTION indicates a hazard to property including the product.

The following symbol(s) may appear on the product:

Service safety summary

Only qualified personnel should perform service procedures. Read this *Service safety summary* and the *General safety summary* before performing any service procedures.

Do not service alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use care when servicing with power on. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Compliance information

This section lists the EMC (electromagnetic compliance), safety, and environmental standards with which the instrument complies.

Environmental considerations

This section provides information about the environmental impact of the product.

Product end-of-life handling

Observe the following guidelines when recycling an instrument or component:

Equipment recycling. Production of this equipment required the extraction and use of natural resources. The equipment may contain substances that could be harmful to the environment or human health if improperly handled at the product's end of life. To avoid release of such substances into the environment and to reduce the use of natural resources, we encourage you to recycle this product in an appropriate system that will ensure that most of the materials are reused or recycled appropriately.

This symbol indicates that this product complies with the applicable European Union requirements according to Directives 2002/96/EC and 2006/66/EC on waste electrical and electronic equipment (WEEE) and batteries. For information about recycling options, check the Support/Service section of the Tektronix Web site (www.tektronix.com).

Restriction of hazardous substances

This product is classified as Monitoring and Control equipment, and is outside the scope of the 2002/95/EC RoHS Directive.

Preface

This document provides information on using and servicing the P5960 logic analyzer probe.

Related documentation

The following list and table provide information on the related documentation available for your Tektronix product. For additional information, refer to the Tektronix Web site (www.tektronix.com/manuals).

Related documentation

Item	Purpose
TLA Quick Start User Manuals	High-level operational overview
Online Help	In-depth operation and UI help
Installation Reference Sheets	High-level installation information
Installation Manuals	Detailed first-time installation information
XYZs of Logic Analyzers	Logic analyzer basics
Declassification and Securities instructions	Data security concerns specific to sanitizing or removing memory devices from Tektronix products
Application notes	Collection of logic analyzer application specific notes
Product Specifications & Performance Verification Procedures	TLA Product specifications and performance verification procedures
TPI.NET Documentation	Detailed information for controlling the logic analyzer using .NET
Field upgrade kits	Upgrade information for your logic analyzer
Optional Service Manuals	Self-service documentation for modules and mainframes

Operating basics

This section provides a brief description of the Tektronix P5960 High-Density Logic Analyzer Probe, information on attaching color-coded probe labels, and probe and adapter connection instructions from the logic analyzer to the SUT.

Product description

The P5960 Probe is a 34-channel, high-density connectorless probe with D-Max probing technology.

The P5960 Probe consists of one probe head that has 34 channels (32 data and 2 clock/qual). (See Figure 1.)

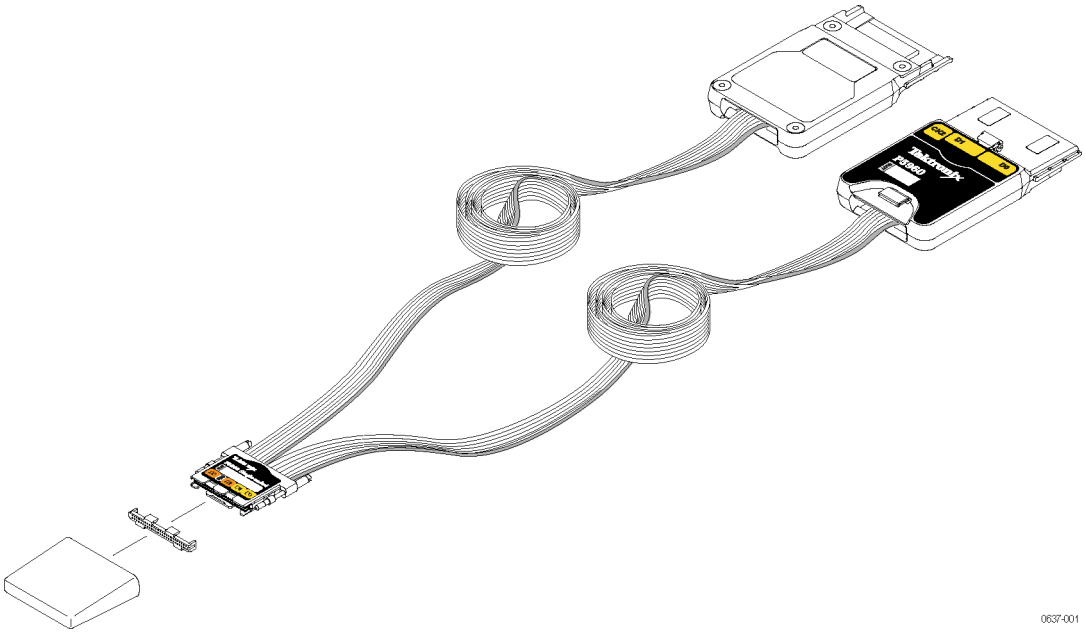


Figure 1: P5960 High-Density probe with D-Max probing technology

The following list details the capabilities and qualities of the P5960 probe:

- Single-ended data and single-ended clock inputs
- cLGA contact eliminates need for built-in connector
- Footprint supports direct signal pass-through
- Supports PCB thickness of 1.27 mm to 6.35 mm (0.050 in to 0.250 in)
- Consists of one independent probe head of 34 channels (32 data and 2 clock/quals), and two 17-channel logic analyzer-end connectors.
- Half channel demux mode, (for example, 1:2 demultiplexing) uses one-half of the probe head

- Color-coded keyed attachment
- -2.5 V to +5 V input operating range
- 300 mV minimum single-ended signal amplitude
- Minimal loading of 20 kΩ, 0.8 pF to ground

P5960 probe accessory information

The P5960 probe includes accessories to connect the logic analyzer to the SUT.

The following accessories are available for the P5960 probe:

- Component kit cLGA interface clip kit (Tektronix part number, 020-2622-xx)
- Primary probe retention kit (Tektronix part number, 020-2908-xx); includes two retention assembly sockets and manual
- Probe labels, one sheet (Tektronix part number, 335-2737-xx)
- *P5960 Logic Analyzer Probe Instructions* (Tektronix part number, 071-2976-xx)
- *P5960 High-Density Logic Analyzer Probe Instruction Manual* (Tektronix part number, 077-0637-xx, available on the TLA Documentation CD or downloadable from the Tektronix Web site: www.tektronix.com/manuals)

Probe label overview

The logic analyzer probe comes with a sheet of labels to apply to the probe before connecting the probe to the instrument and SUT.

When you purchase the logic analyzer probe, apply the color-coded labels as described in this section. The labels help you identify the probe connections at the logic analyzer end and at the SUT end.

The following table lists the probe section and label color combinations. Refer to the table when you attach the probe labels.

Table 1: Probe section and label combinations

Probe section	Channels	Label color	Probe section	Channels	Label color
A3-A2	CK0, A3:7-0, A2:7-0	Brown	A1-A0	CK1, A1:7-0, A0:7-0	Orange
D3-D2	QUAL0, D3:7-0, D2:7-0	Blue	D1-D0	CK2, D1:7-0, D0:7-0	Yellow
C3-C2	CK3, C3:7-0, C2:7-0	White	C1-C0	QUAL1, C1:7-0, C0:7-0	Gray
E3-E2	QUAL3, E3:7-0, E2:7-0	Green	E1-E0	QUAL2, E1:7-0, E0:7-0	Violet

The following figure shows a sample probe label sheet.

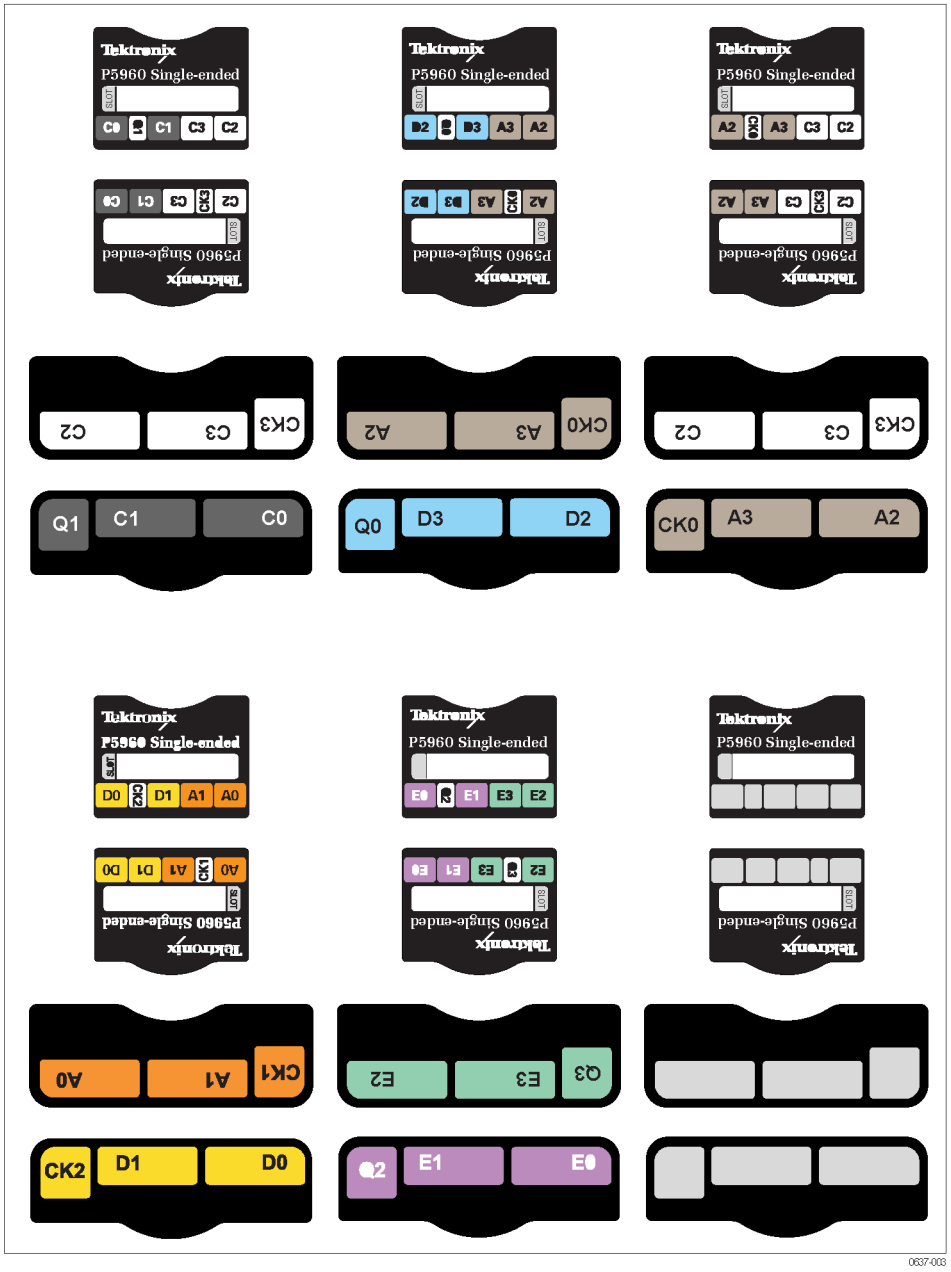


Figure 2: P5960 probe label sheet.

Apply the labels to the probe

Attach the labels to the logic analyzer-end of the probe and to both sides of the probe head.

NOTE. *Use flat-nosed tweezers to remove the labels from the sheet of labels. Never peel labels with your fingers. The labels are made of soft vinyl and can stretch and distort easily. To avoid stretching the label, always hold it from the top right corner while removing it from the sheet of labels.*

The adhesive on the vinyl labels is extremely strong. Carefully align each label to the intended outline on the logic analyzer-end and probe head before attaching it to the probe. Once labels are placed on the probe, they become very difficult to remove.

Use the following steps to attach the probe labels:

1. Identify the logic analyzer-ends of the probes.

   The side of the probe that contains a black label has an area for the color-coded label.

NOTE. *Note the indents and the outdents on the probe labels. Use the indents and outdents as guides to position the labels on the probes. (See Figure 3 on page 6.)*

2. From the sheet of labels, locate the color-coded label for the logic analyzer end of the probe cable and attach it to the logic analyzer probe connector.
3. Locate the probe head and attach the matching colored label to the probe head.(See Figure 3 on page 6.)
4. Turn the probe over and repeat Step 3 to apply the other labels to the probe as shown in the illustration.

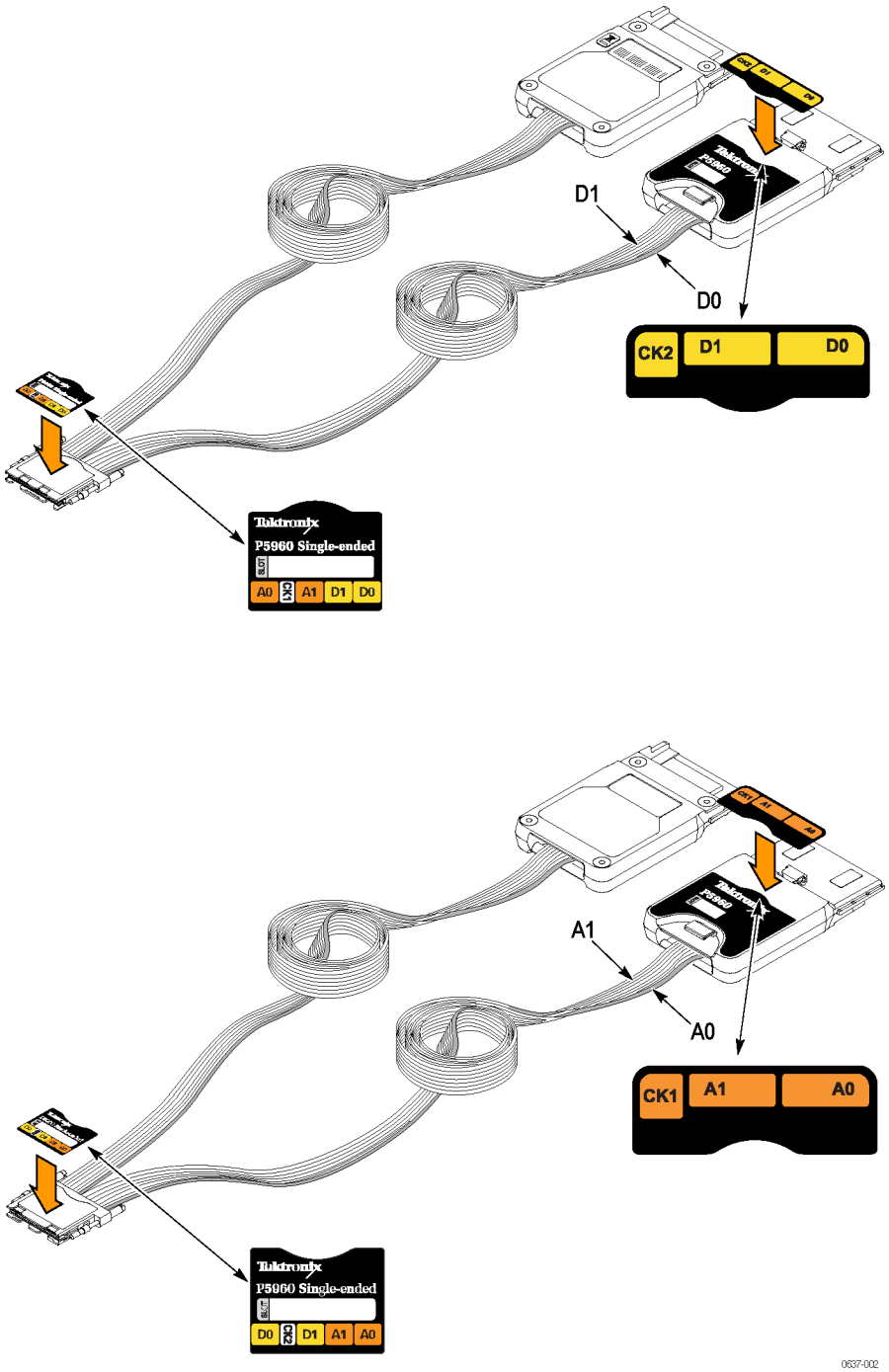


Figure 3: Attaching labels to the P5960 probe

Probe connection overview

The P5960 probe connects a TLA6400 Series logic analyzer to probe retention assemblies installed on the circuit board on the SUT.

If the retention assemblies are not already installed on the SUT, refer to the procedures for installing the retention assemblies. (See page 37, *Probe retention assembly installation information*.)

Probe head handling guidelines

The cLGA interface clip in the probe head should always be handled with care.

Use the following guidelines when you handle the probe head and cLGA interface clip:

- Always handle the cLGA interface clip by the outer edges, and be careful to avoid the contacts in the center. Do not touch the contacts with your fingers, tools, wipes, or any other devices. (See Figure 4.)

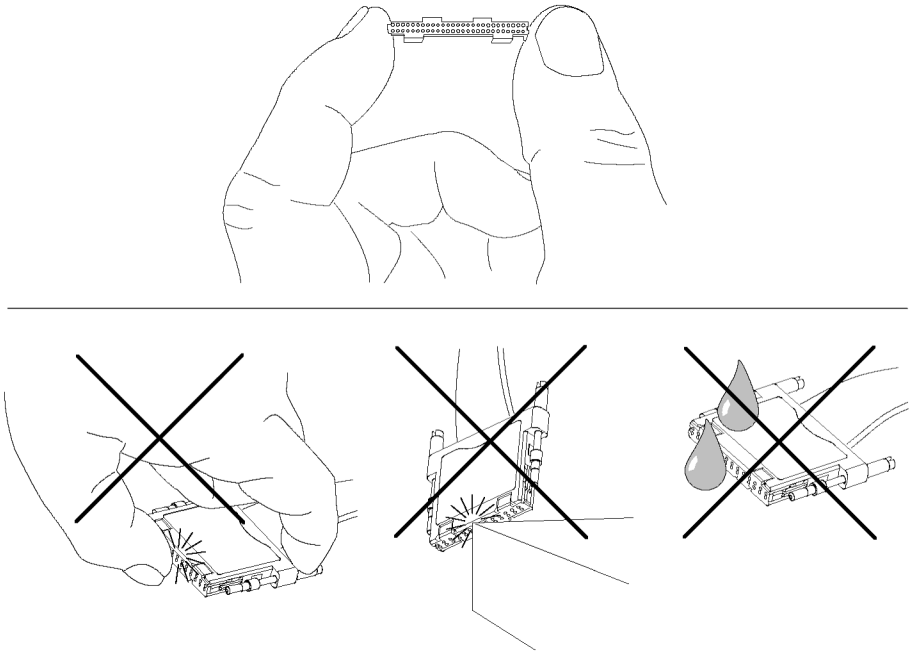


Figure 4: Proper handling of the interface clip

- Do not expose the connector to liquids or dry chemicals.
- If the board pad array needs to be cleaned, only use isopropyl alcohol and lint-free cloth. (See page 37, *Clean the compression footprints on the SUT*.)
- Immediately following cleaning, or immediately prior to placement of connector to circuit board, blow off the board pad array and connector contact array with clean, oil-free dry air or nitrogen to remove loose debris. First start

the blowing process by aiming away from the array areas, and then sweep across the pad and contact arrays in a repeated motion to remove loose debris.

- Place the connector onto the board pad array using the bosses or locator pins for alignment. Use care to prevent incidental contact with other surfaces or edges in the connector contact array area prior to board placement.
- Always store the probe head in the protective cover when not in use. (See Figure 5.)

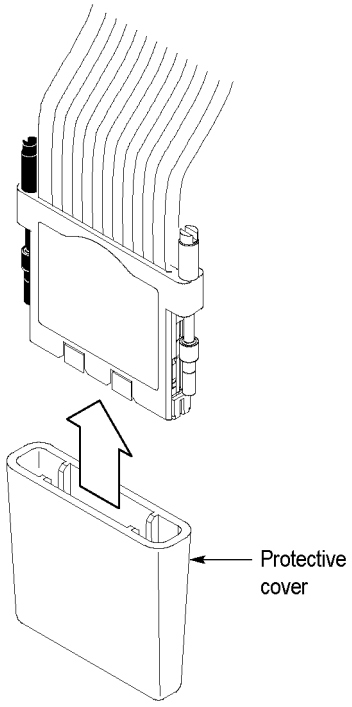


Figure 5: Storing the probe head

Connect the probe to the instrument

The P5960 probe connects a TLA6400 Series logic analyzer to the SUT. You can connect the P5960 probe to the SUT without turning off the power to the SUT.

Apply the labels to the probes before connecting the probes to the instrument and to the SUT.

1. Match the color-coded labels of the probe to the same color-coded connector on the logic analyzer.
2. Connect the logic analyzer probe as shown. The probe will latch into place.

   To disconnect the probe, press the button at the center of the probe to release the latch and then pull the probe away from the logic analyzer.

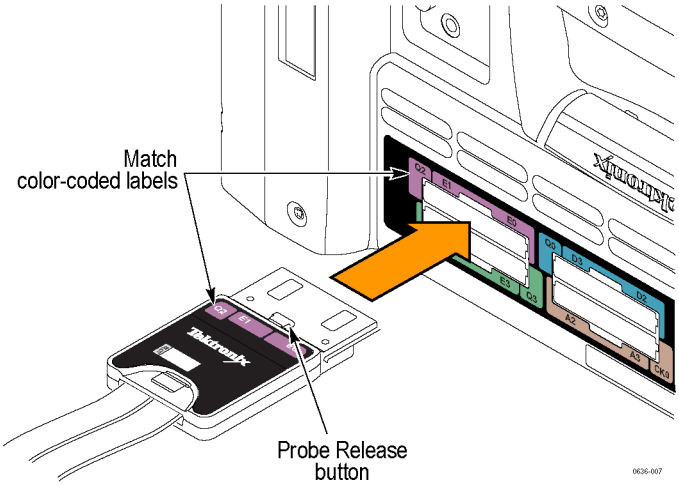


Figure 6: Connecting the logic analyzer probe

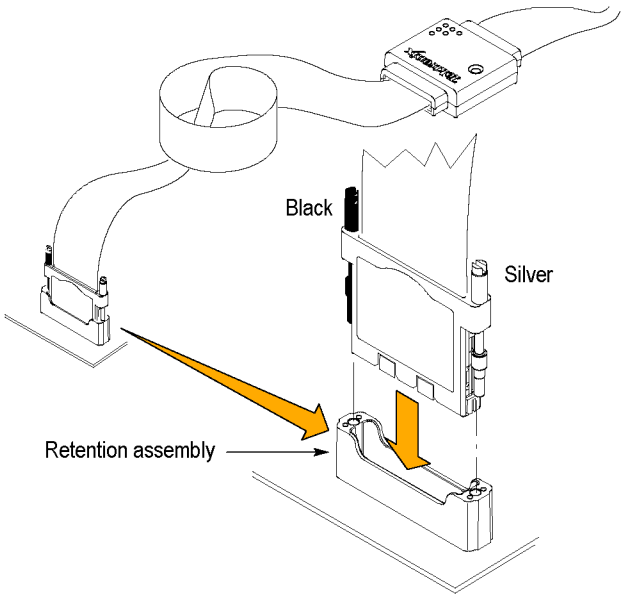
Connect the probes to the SUT

The probe heads connect to the retention assembly on the SUT.

Verify that one or more retention assemblies are installed on the SUT before you attempt to connect the probes. If they are not installed refer to the instructions for installing them. (See page 37, *Install the probe retention assembly*.)

Connect the probes to the SUT using the following steps.

1. Align the silver screw on the probe to the silver side of the retention assembly.



Note: The retention assembly is visually keyed (one side is black and one side is silver).

Figure 7: Connecting the probes to the SUT

2. Start both screws in the retention assembly, and tighten them evenly (approximately 1 in-lb) to make sure that the probe approaches and mates squarely to the circuit board.

CAUTION. *When attaching the probe head to the target system, use care to evenly tighten probe head screws until they are snug. First tighten both screws until the nut bar makes contact with the circuit board surface, then snug each screw to 1 in-lb (max). Under-tightening the probe head screws can result in intermittence. Over-tightening can result in damage to the cLGA clip and stripped screws.*

If access is limited, use the adjustment tool that came with your probe. The probe is completely fastened when the screws stop in the assembly.

Dress the probe cables

Use the Velcro cable managers to combine the cables together or to help relieve strain on the probe connections.

Hang the probe cables so that you relieve the tension on the probes at the retention posts as shown in the following figure.

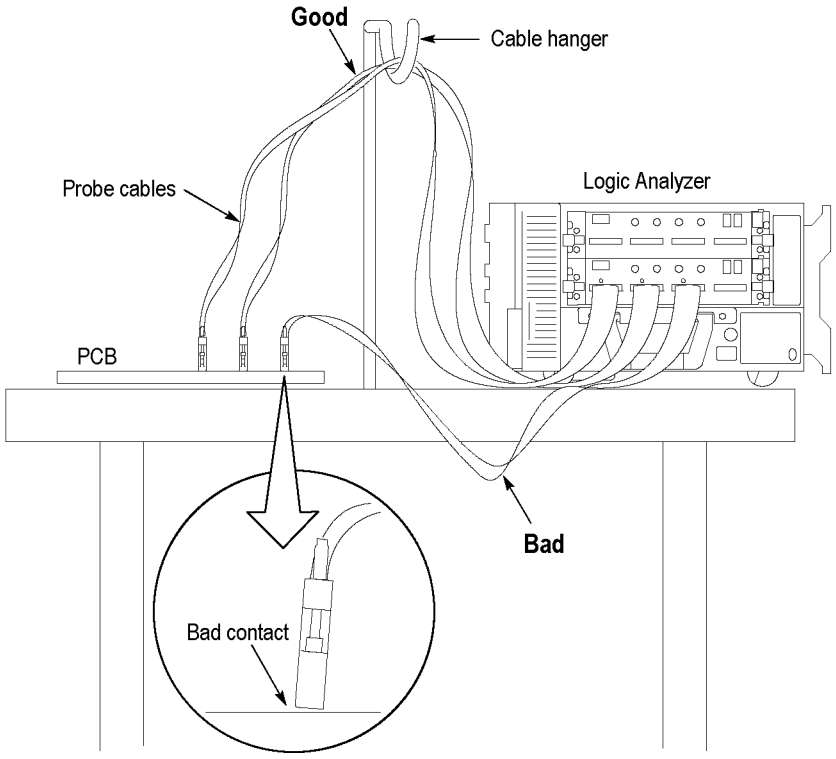


Figure 8: Proper dressing of the probe cables

Store the probe head when not in use

To protect the interface clip, it is important to properly store the probe head when the probe is not in use. Use the protective cover as shown in the following figure.

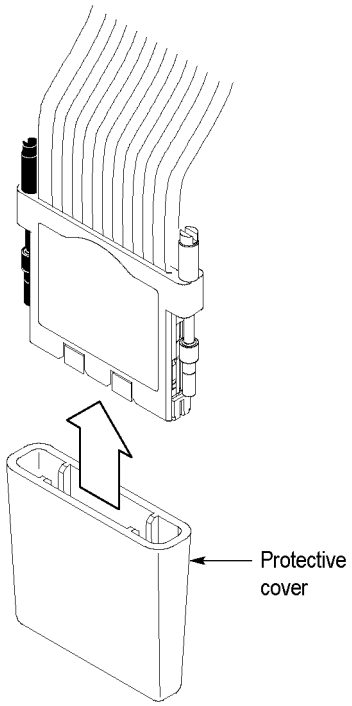


Figure 9: Protecting the probe head

Probe connection troubleshooting guidelines

Refer to the guidelines in this section to identify probe connection problems.

The most obvious symptom of a problem with the probe installation is seeing incorrect data in the logic analyzer acquisition. The nature of the incorrect data has a very consistent characteristic; the data from multiple channels go to a logic low and stay there. Intermittent bad data, or a single dead channel are not failures typically associated with probe installation problems.

- Slightly move the probe head to either side, or press down on the probe head while making new acquisitions.

  If good data is now being acquired, then the probe mounting is most likely the cause.

- If good data is not acquired, then remove the probe and check the retention assembly for too much play.

  If there is significant play, then the probe mounting is most likely the cause.

- If the retention assembly has minimal play and you cannot see a gap between the bottom of the assembly and the circuit board surface, then move the probe with bad data from one logic analyzer probe location to another.

  If the problem follows the probe, then the probe is the problem.

- Visually inspect the cLGA interface clip on the probe for any damage or missing c-spring metal contacts.

  If there is damage to the interface clip, or if any c-spring metal contacts are missing, replace the cLGA interface clip. (See page 32, *Replace the cLGA clip*.)

- If the problem does not follow the probe, it is either the logic analyzer or the probe connection at its previous location.

  Move the probe back to the original location to be certain it was not a connection problem at the logic analyzer end.

- Place another probe in the retention assembly of the original probe. If the new probe acquires data, then the old probe is probably at fault.

Reference

This section provides reference information for the P5960. After you have determined which probe is required, use the information in this section to design the appropriate connector into your SUT circuit board.

Clocks and qualifiers

Use the clock and qualifier probe connections from the SUT to define how the logic analyzer stores data.

Every logic analyzer has some special purpose input channels. Inputs designated as clocks can cause the logic analyzer to store data. Qualifier channels can be logically ANDed and ORed with clocks to further define when the logic analyzer should latch data from the SUT. Routing the appropriate signals from your design to these inputs ensures that the logic analyzer can acquire data correctly. Unused clocks can be used as qualifier signals.

Depending on the channel width, each TLA6400 Series logic analyzer will have a different set of clock and qualifier channels. The following table shows the clock and qualifier channels available for each instrument.

Table 2: Logic analyzer clock and qualifier availability

Product	Clock inputs				Qualifier inputs			
	CLK:0	CLK:1	CLK:2	CLK:3	QUAL:0	QUAL:1	QUAL:2	QUAL:3
TLA6401	X			X				
TLA6402	X	X	X	X				
TLA6403	X	X	X	X	X	X		
TLA6404	X	X	X	X	X	X	X	X

All clock and qualifier channels are stored. The logic analyzer always stores the logic state of these channels every time it latches data.

Since clock and qualifier channels are stored in the logic analyzer memory, there is no need to double probe these signals for timing analysis. When switching from state to timing analysis, all of the clock and qualifier signals are visible. This allows you to route signals not needed for clocking to the unused clock and qualifier channels.

It is a good practice to take advantage of the unused clock and qualifier channels to increase your options for when you will latch data. Routing several clocks and strobes in your design to the logic analyzer clock inputs will provide you with a greater flexibility in the logic analyzer Setup menu.

As an example, look at a processor with a master clock, data strobe, and an address strobe. Routing all three of these signals to logic analyzer clock inputs will enable you to latch data on the processor master clock, only when data is strobed, or only when address is strobed. Some forethought in signal routing can greatly expand the ways to latch and analyze data.

A processor also provides a good example of signals that can be useful as qualifiers. There are often signals that indicate data reads versus data writes (R/W), signals that show when alternate bus masters have control of the processor buses (DMA), and signals that show when various memory devices are being used (ChipSel). All of these signals are good candidates for assignment to qualifier channels.

By logically ANDing the clock with one of these qualifiers you can program the logic analyzer to store only data reads or data writes. Using the DMA signal as a qualifier provides a means of filtering out alternate bus master cycles. Chip selects can limit data latching to specific memory banks, I/O ports, or peripheral devices.

Multiplexed buses

TLA6400 Series logic analyzers support half channel demultiplexing.

Each signal on a dual multiplexed bus can be demultiplexed into its own logic analyzer channel. See the following table to determine the correct channel groups to use.

Table 3: Half channel demultiplexing source-to channel assignments

Source connecting channel groups	Destination channels receiving SUT test data			
	TLA6404	TLA6403	TLA6402	TLA6401
A3:7-0	D3:7-0	D3:7-0		
A2:7-0	D2:7-0	D2:7-0		
A1:7-0	D1:7-0	D1:7-0	D1:7-0	
A0:7-0	D0:7-0	D0:7-0	D0:7-0	
C3:7-0	C1:7-0	C1:7-0	A3:7-0	A3:7-0
C2:7-0	C0:7-0	C0:7-0	A2:7-0	A2:7-0
E3:7-0	E1:7-0			
E2:7-0	E0:7-0			

When demultiplexing data there is no need to connect the destination channels to the multiplexed bus. Data from the source channels are routed to the destination channels internal to the logic analyzer.

Demultiplexing affects only the main memory for the destination channels. This means that the MagniVu memory is filled with data from whatever is connected to the demultiplexing destination channel probe inputs. This provides an opportunity to acquire high resolution MagniVu data on a few extra channels. Connecting the demultiplexing destination channels to other signals will allow viewing of their activity in the MagniVu memory but not the main memory.

High-Resolution timing

The high-resolution timing mode provides double the normal 800 MHz sample rate on one-half of the channels. By trading half of the channels, the remaining channels can be sampled at a 1.6 GHz rate with double the memory depth.

Obtain extra timing resolution where it is most needed by assigning critical signals to the demultiplexing source channels. Since demultiplexing affects only the main memory you will still have the MagniVu data available for all of the signals that are disconnected from the main memory when you switch to the high resolution timing modes.

Range recognizers

When using range recognizers, the probe groups and probe channels must be in hardware order.

Probe groups must be used from the most-significant probe group to the least-significant probe group based on the following order:

```
C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0
CK3 CK2 CK1 CK0
```

Probe channels must be from the most-significant channel to the least-significant channel based on the following order:

```
7 6 5 4 3 2 1 0
```

The above examples assumes a 136-channel logic analyzer. The missing channels in logic analyzers with fewer than 136 channels are ignored.

Probe dimensions

The following figure shows the dimensions for the P5960 probe.

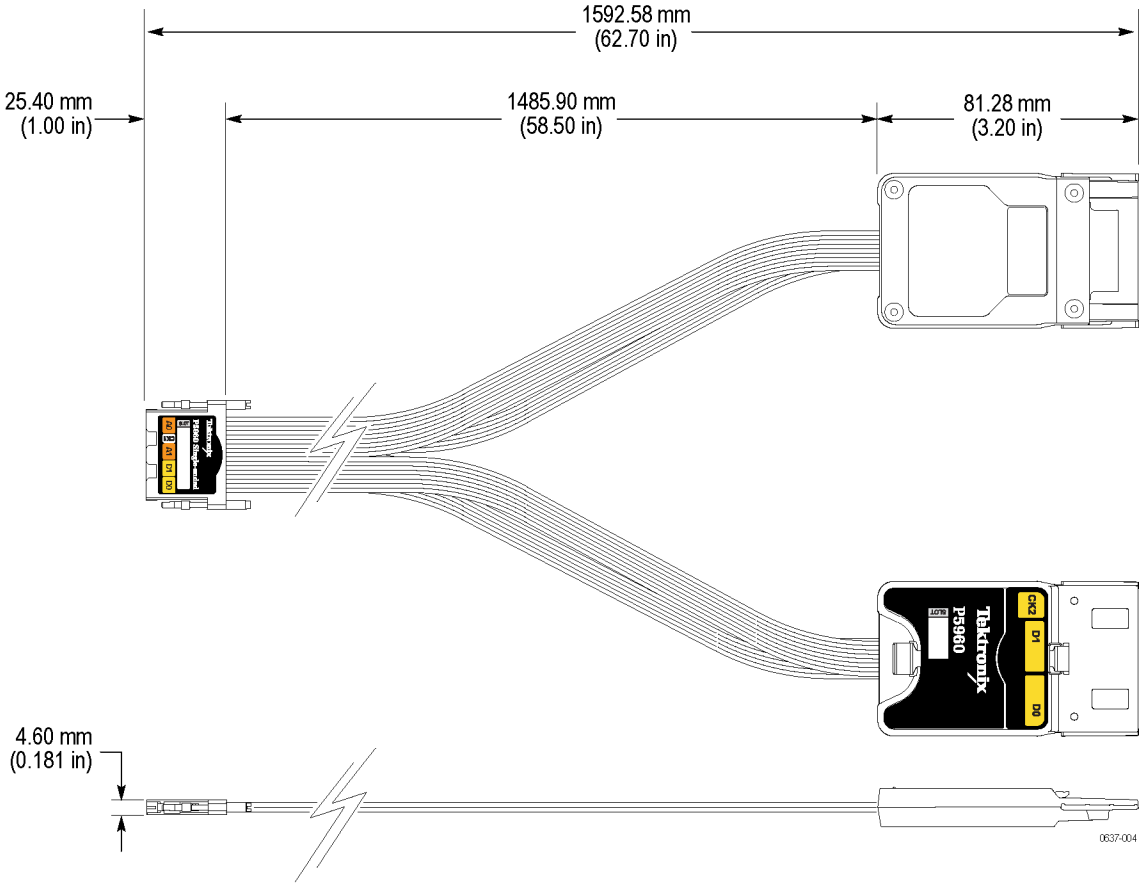


Figure 10: P5960 probe dimensions

Retention assembly dimensions and keepout areas

The retention assembly provides a housing around the probe connector footprint to stabilize the probe. The following figure shows the dimensions of the retention assembly. All dimensions are per standard IPC tolerance, which is ±0.004 in. (See Figure 11.)

CAUTION. *To avoid solder creep, bend the assembly wires out after you insert the wires in the board, and then solder the wires.*

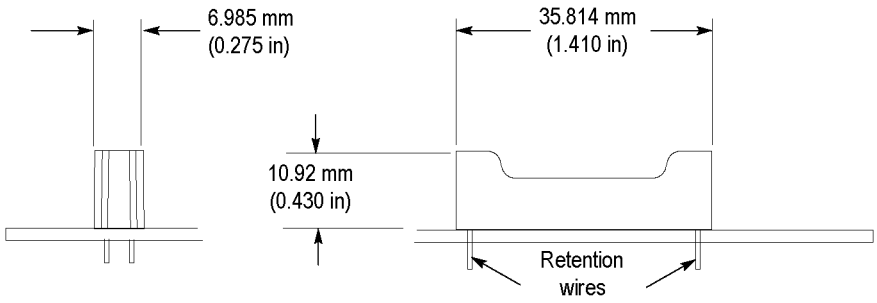


Figure 11: Retention assembly dimensions

The following figure shows the keep out area required for the retention assembly.

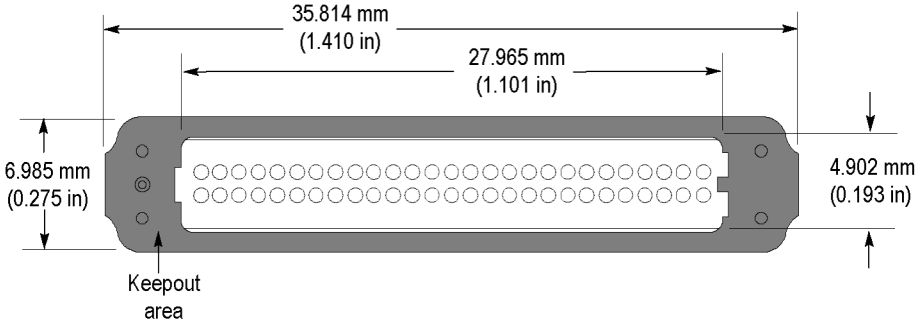


Figure 12: Retention assembly keepout area

NOTE. *Tektronix has provided a 3D CAD solid model file (named dmax_socket_assembly.stp) for the plastic retention assembly. It also includes footprint information for your circuit board. The file is attached to this PDF file. To access the attached file, open the PDF file and click on the paperclip icon on the left side of the document viewer.*

Retention assembly side-by-side and end-to layout dimensions

The following figure shows the dimensions for side-by-side footprint layout. (See Figure 17.)

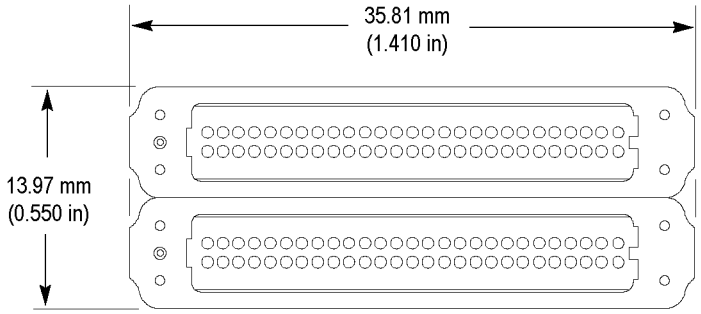


Figure 13: Retention assembly side-by-side layout

The following figure shows the dimensions for an end-to-end footprint layout.

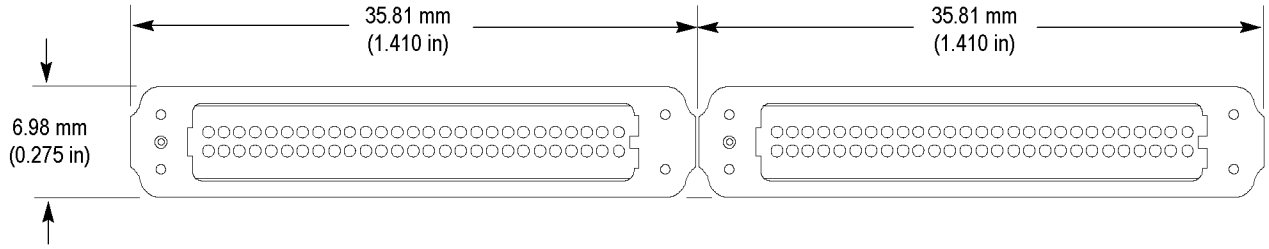


Figure 14: Retention assembly end-to-end layout

Retention post dimensions and keepout areas

Retention posts provide another means for attaching the probes to the PCB. the retention posts hold the probe securely to the board, and ensure a reliable electrical and mechanical connection and pin-to-pad alignment to your design. Board thicknesses that are supported include 1.27 mm (0.050 in) to 6.35 mm (0.250 in). The dimensions of the retention posts are shown in the following figure. (See Figure 15.)

All dimensions are per standard IPC tolerance, which is ±0.004 in.

CAUTION. *To avoid solder creep, bend the post wires out after you insert the posts in the board, and then solder the post wires. You can solder the retention wires from the top or bottom of the circuit board.*

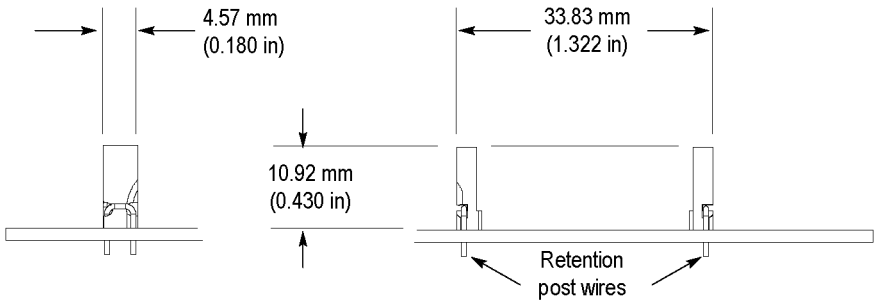


Figure 15: Retention posts dimensions

The following figure shows the keepout area required for the retention posts. (See Figure 16.) Vias must be placed outside of the keepout area. Any traces routed on the top layer of the board must stay outside of the keepout area. Traces can be routed on inner layers of the board through the keepout area.

Figure 16: Retention posts keepout area

Retention post side-by-side and end-to-end layout dimensions

The following figure shows the dimensions for side-by-side footprint layout. (See Figure 17.)

Figure 17: Retention posts side-by-side layout

The following figure shows the dimensions for an end-to-end footprint layout. (See Figure 18.)

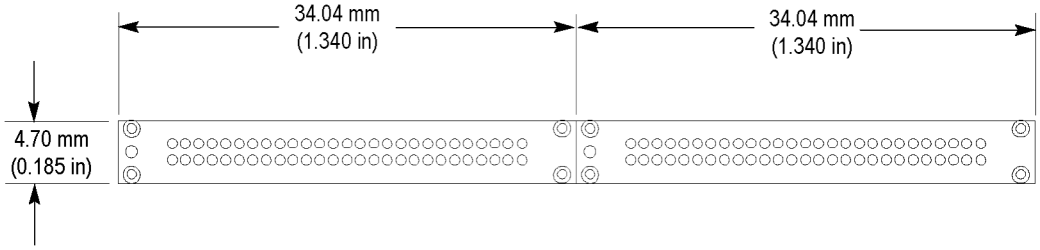


Figure 18: Retention posts end-to-end layout

Signal routing

The following figure shows examples of pass-through signal routing for a single-ended data configuration.

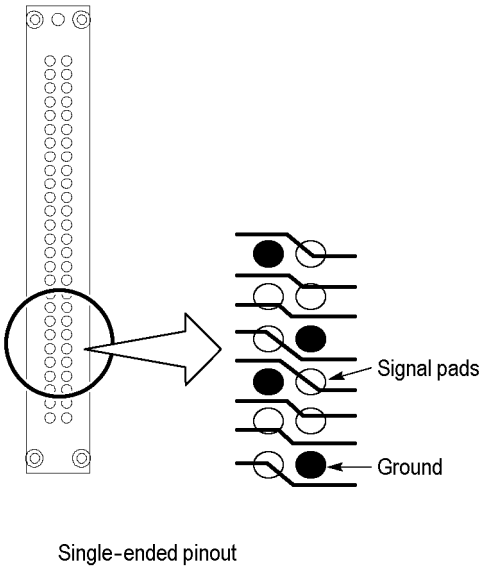


Figure 19: Signal routing on the SUT

Mechanical considerations

The PCB holes, in general, do not have an impact upon the integrity of your signals when the signals routed around the holes have the corresponding return current plane immediately below the signal trace for the entire signal path from driver to receiver.

NOTE. *For optimum signal integrity, there should be a continuous, uninterrupted ground return plane along the entire signal path.*

Electrical considerations

Load models are important electrical considerations when working with the probe.

The compression land pattern pad is not part of the load model. Make sure that you include the compression land pad in the modeling.

Transmission lines

Due to the high performance nature of the interconnect, make sure that stubs, which are greater than 1/4 length of the signal rise time, are modeled as transmission lines.

P5960 probe load model

The following electrical model includes a low-frequency model of the High-Density Single-Ended Probe.

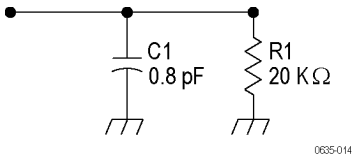


Figure 20: High-Density probe load model

Probe footprint dimensions

Use the probe footprint dimensions to lay out your circuit board pads and holes for attaching the retention posts.

(See Figure 21 on page 25.) If you are using the alternate retention assembly, all dimensions remain the same as shown below, except the overall length and width. (See Figure 11 on page 19.) Pad finishes that are supported include immersion gold, immersion silver, and hot air solder level.

All dimensions are per standard IPC tolerance, which is ±0.004 in.

NOTE. *Tektronix recommends using immersion gold surface finish for best performance.*

Tektronix also recommends that the probe attachment holes float or remain unconnected to a ground plane. This prevents overheating the ground plane and promotes quicker soldering of the retention posts to your PCB. The probe retention posts are designed to allow you to solder the retention posts from either side of your PCB.

NOTE. *Tektronix has provided a 3D CAD solid model file (named dmax_socket_assembly.stp) for the plastic retention assembly. It also includes footprint information for your circuit board. The file is attached to this PDF file. To access the attached file, open the PDF file and click on the paperclip icon on the left side of the document viewer.*

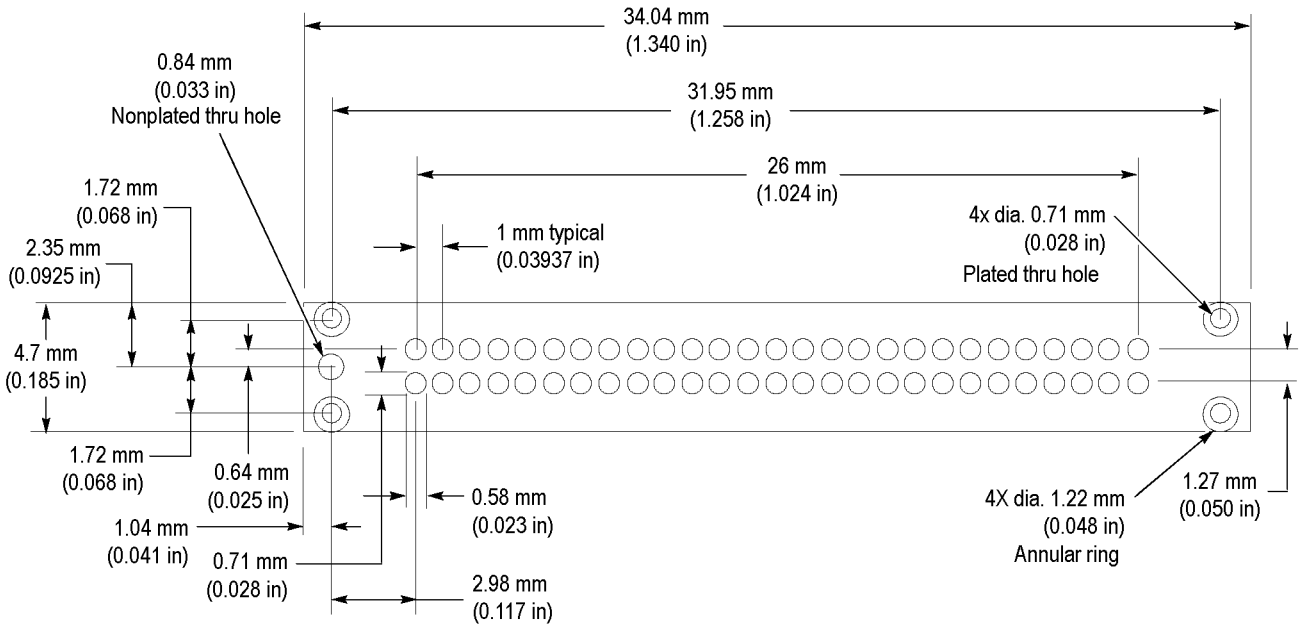


Figure 21: Probe footprint dimensions on the PCB

NOTE. *Maintain a solder mask web between the pads when traces are routed between pads on the same layer. The solder mask must not encroach onto the pads within the pad dimensions. (See Figure 16 on page 21.)*

Via-in-Pad design considerations

Traditional layout techniques require vias to be located next to a pad and a signal routed to the pad causing a stub and more PCB board area to be used for the connection.

Many new digital designs require you to minimize the electrical effects of the logic analyzer probing that you design into the circuit board. Using via-in-pad to route signals to the pads on the circuit board allows you to minimize the stub length of the signals on your board, thus providing the smallest intrusion to your signals. It also enables you to minimize the board area that is used for the probe footprint and maintain the best electrical performance of your design.

The following figure shows a footprint example where two pads use vias. Detail A describes the recommended position of the via with respect to the pad.

All dimensions are per standard IPC tolerance, which is ±0.004 in.

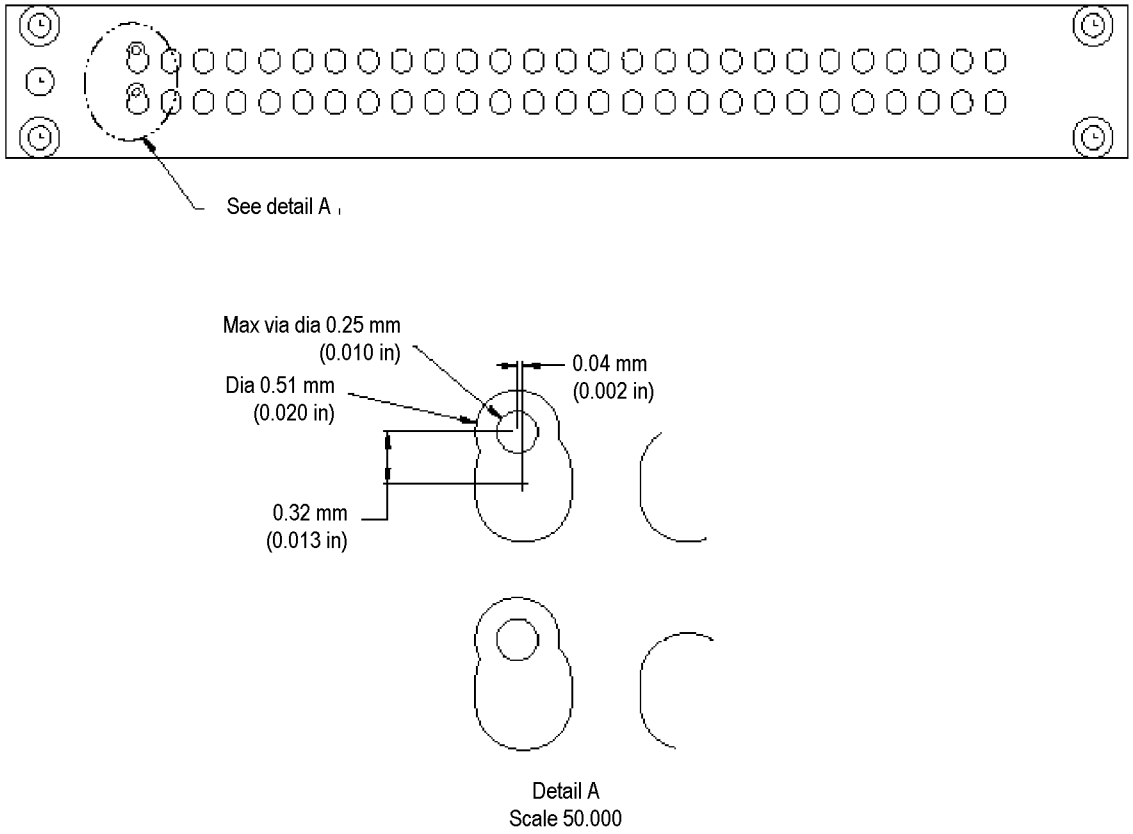


Figure 22: Optional Via-in-Pad placement recommendation

Probe pinout definition and channel assignment

Probe pinout definitions and channel assignments provide useful information for your design for use with the logic analzyer.

The following figure shows the pad assignments, pad numbers, and signal names for the PCB footprint of the P5960 single-ended logic analyzer probe. The P5960 probe has 32 data channels, one clock, and one qualifier for each footprint.

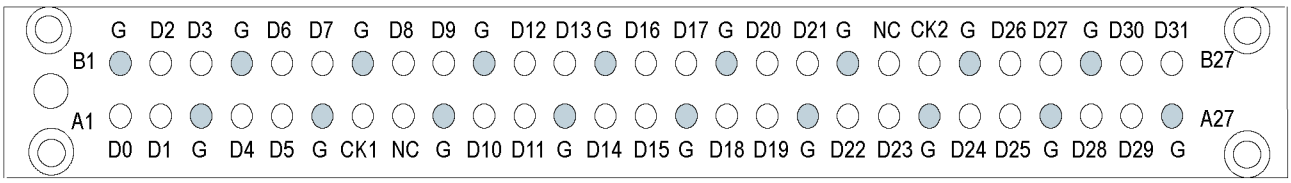


Figure 23: P5960 single-ended PCB footprint pinout detail

The following table lists the channel mapping to a TLA6400 Series logic analyzer for a P5960 single-ended logic analyzer probe.

Table 4: Channel assignment for a P5960 single-ended logic analyzer probe

Number of channels		136	136 or 102	136 or 102	136 or 102	68	68 or 34
Pin	**Signal**	**Probe4**	**Probe 3**	**Probe 2**	**Probe 1**	**Probe 2**	**Probe 1**
A1	D0	E2:0	A2:0	A0:0	C2:0	A0:0	C2:0
A2	D1	E2:1	A2:1	A0:1	C2:1	A0:1	C2:1
A3	GND	GND	GND	GND	GND	GND	GND
A4	D4	E2:4	A2:4	A0:4	C2:4	A0:4	C2:4
A5	D5	E2:5	A2:5	A0:5	C2:5	A0:5	C2:5
A6	GND	GND	GND	GND	GND	GND	GND
A7	CK1	Q3	CK0	CK1	CK3	CK1	CK3
A8	NC	NC	NC	NC	NC	NC	NC
A9	GND	GND	GND	GND	GND	GND	GND
A10	D10	E3:2	A3:2	A1:2	C3:2	A1:2	C3:2
A11	D11	E3:3	A3:3	A1:3	C3:3	A1:3	C3:3
A12	GND	GND	GND	GND	GND	GND	GND
A13	D14	E3:6	A3:6	A1:6	C3:6	A1:6	C3:6
A14	D15	E3:7	A3:7	A1:7	C3:7	A1:7	C3:7
A15	GND	GND	GND	GND	GND	GND	GND
A16	D18	E1:5	D3:5	D1:5	C1:5	D1:5	A3:5
A17	D19	E1:4	D3:4	D1:4	C1:4	D1:4	A3:4
A18	GND	GND	GND	GND	GND	GND	GND
A19	D22	E1:1	D3:1	D1:1	C1:1	D1:1	A3:1
A20	D23	E1:0	D3:0	D1:0	C1:0	D1:0	A3:0

Table 4: Channel assignment for a P5960 single-ended logic analyzer probe (cont.)

Number of channels		136	136 or 102	136 or 102	136 or 102	68	68 or 34
Pin	**Signal**	**Probe4**	**Probe 3**	**Probe 2**	**Probe 1**	**Probe 2**	**Probe 1**
A21	GND	GND	GND	GND	GND	GND	GND
A22	D24	E0:7	D2:7	D0:7	C0:7	D0:7	A2:7
A23	D25	E0:6	D2:6	D0:6	C0:6	D0:6	A2:6
A24	GND	GND	GND	GND	GND	GND	GND
A25	D28	E0:3	D2:3	D0:3	C0:3	D0:3	A2:3
A26	D29	E0:2	D2:2	D0:2	C0:2	D0:2	A2:2
A27	GND	GND	GND	GND	GND	GND	GND
B1	GND	GND	GND	GND	GND	GND	GND
B2	D2	E2:2	A2:2	A0:2	C2:2	A0:2	C2:2
B3	D3	E2:3	A2:3	A0:3	C2:3	A0:3	C2:3
B4	GND	GND	GND	GND	GND	GND	GND
B5	D6	E2:6	A2:6	A0:6	C2:6	A0:6	C2:6
B6	D7	E2:7	A2:7	A0:7	C2:7	A0:7	C2:7
B7	GND	GND	GND	GND	GND	GND	GND
B8	D8	E3:0	A3:0	A1:0	C3:0	A1:0	C3:0
B9	D9	E3:1	A3:1	A1:1	C3:1	A1:1	C3:1
B10	GND	GND	GND	GND	GND	GND	GND
B11	D12	E3:4	A3:4	A1:4	C3:4	A1:4	C3:4
B12	D13	E3:5	A3:5	A1:5	C3:5	A1:5	C3:5
B13	GND	GND	GND	GND	GND	GND	GND
B14	D16	E1:7	D3:7	D1:7	C1:7	D1:7	A3:7
B15	D17	E1:6	D3:6	D1:6	C1:6	D1:6	A3:6
B16	GND	GND	GND	GND	GND	GND	GND
B17	D20	E1:3	D3:3	D1:3	C1:3	D1:3	A3:3
B18	D21	E1:2	D3:2	D1:2	C1:2	D1:2	A3:2
B19	GND	GND	GND	GND	GND	GND	GND
B20	NC	NC	NC	NC	NC	NC	NC
B21	CK2	Q2	Q0	CK2	Q1	CK2	CK0
B22	GND	GND	GND	GND	GND	GND	GND
B23	D26	E0:5	D2:5	D0:5	C0:5	D0:5	A2:5
B24	D27	E0:4	D2:4	D0:4	C0:4	D0:4	A2:4
B25	GND	GND	GND	GND	GND	GND	GND
B26	D30	E0:1	D2:1	D0:1	C0:1	D0:1	A2:1
B27	D31	E0:0	D2:0	D0:0	C0:0	D0:0	A2:0

Specifications

The following tables list the electrical and environmental specifications for the P5910 probe.

The electrical specifications apply when the probe is connected between a compatible logic analyzer and the SUT. Refer to the *Tektronix TLA6400 Logic Analyzer Product Specifications & Performance Verification* document (available on the *Tektronix Logic Analyzer Family Product Documentation* CD or downloadable from the Tektronix Web site) for a complete list of specifications, including overall system specifications.

Table 5: Mechanical and electrical specifications

Characteristic	P5960
Number of input channels	34, (32 data channels, 2 clock/qualifier channels)
Input impedance	20 kΩ, 0.8 pF to ground
Analog bandwidth	2 GHz
Minimum input signal	300 mV_{p-p}
Operating signal range	-2.5 V to 5 V
Maximum nondestructive input signal to probe	-4.5 V to +13 V
Channel to channel skew	±60 ps, within a single probe ±125 ps, between probes
Delay from probe tip to input connector	6.39 ns
Probe length (including probe head and probe connector)	1.593 m (62.7 in)

The following table lists environmental specifications for the probe. The probe is designed to meet Tektronix standard 062-2847-00.

Table 6: Environmental specifications

Characteristic	P59xx
Temperature	
Operating	-10 °C to +55 °C (14 °F to +131 °F)
Non-operating	-51 °C to +71 °C (-60 °F to +160 °F)
Humidity	
Operating	5% to 95% relative humidity ≤ 30 °C (86 °F) 5% to 45% relative humidity 30 °C to 55 °C (86 °F to 131 °F), non condensing

Table 6: Environmental specifications (cont.)

Characteristic	P59xx
Non-operating	5% to 95% relative humidity ≤ 30 °C (86 °F) 5% to 45% relative humidity 30 °C to 71 °C (86 °F to 160 °F), non condensing
Altitude Operating	To 3,000 m (9843 ft)
Non-operating	To 12,000 m (39,370 ft)

Maintenance

Probe calibration information

The probe does not require calibration. If a probe failure occurs, return the entire probe to your Tektronix representative for repair.

Probe service strategy information

The following service options are available when you order your Tektronix product:

Table 7: Service options

Option	Description
C3	Calibration Service 3 Years Includes initial certifications plus two annual calibrations
C5	Calibration Service 5 Years Includes initial certifications plus four annual calibrations
R3	Repair Service 3 Years Return product to Tektronix for servicing
R5	Repair Service 5 Years Return product to Tektronix for servicing
R3DW	Repair Service Coverage 3 Years (includes product warranty period). 3-year period starts at time of instrument purchase
R5DW	Repair Service Coverage 5 Years (includes product warranty period). 5-year period starts at time of instrument purchase

Perform the functional check

A functional check verifies basic functionality of the probe.

1. Connect the probe to the logic analyzer and to an active signal source.
2. Open the logic analyzer Setup window.
3. Set the threshold voltage to the appropriate value for the active signal source.
4. Check for signal activity in the Setup window for the attached probe.

Inspect or clean the probe

Inspect and clean the probe as often as operating conditions require. Dirt acts as an insulating blanket, preventing efficient heat dissipation. Dirt also provides an electrical conduction path that can cause failures, especially under high-humidity conditions.

CAUTION. *To prevent damage during the probe connection process, do not touch the exposed edge of the interface clip. Do not drag the contacts against a hard edge or corner.*

Perform the following steps to clean the probe:

1. Keep the probes free of dirt, dust, and contaminants to maintain a reliable electrical probe connection.

   Avoid brushing or rubbing the c-spring contacts.

2. Remove dirt and dust with a soft brush.

3. Use only a damp cloth for more extensive cleaning.

   Never use abrasive cleaners or organic solvents.

Replace the cLGA clip

The P5960 probe uses replaceable c-spring cLGA clips. If a probe failure other than the cLGA clip occurs, return the entire probe to your Tektronix service center for repair.

To replace the cLGA clip, perform the following steps:

1. Gently pull one side of the clip away from the probe head and then remove the entire clip. (See Figure 24.)

2. Align the new clip with the probe head and gently snap it into place.

3. Test the probe to confirm that all channels are functional.

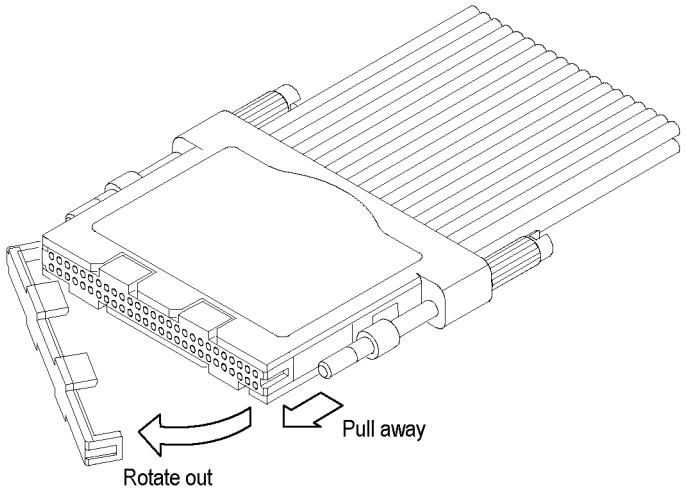


Figure 24: Replacing the cLGA clip

For replacement part number information, refer to the Replaceable Parts list.

Repackage the probe

The following information describes how to repackage the probe, to store the probe, or to return the probes to the factory.

1. Use the original packaging, if possible.

   If the original packaging is not available, use a corrugated cardboard shipping carton.

2. Add cushioning material to prevent the probes from moving inside the shipping container.

3. Enclose the following information when shipping the probe to a Tektronix Center:

   - Owner's address
   - Name and phone number of a contact person
   - Type of probe
   - Reason for return
   - Full description of the service required

Replaceable parts

Parts ordering information

Replacement parts are available through your local Tektronix field office or representative.

The P5960 probe contains no user-replaceable parts. However, probe accessories can be replaced. (See page 2, *P5960 probe accessory information*.) Contact your local Tektronix representative for replacement information.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. When ordering parts, include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in the part number.

Appendix A: Probe retention assembly installation information

The P5960 probes connect to the retention assemblies on the circuit board of the SUT. Two different retention assembles are available: a single piece retention assembly, and a two-piece post assembly (for connecting a probe with limited space on the SUT. This appendix describes the procedures for installing both retention assemblies.

Clean the compression footprints on the SUT

To provide good electrical contacts, clean the compression footprints before installing the retention assemblies on the SUT.

CAUTION. *To avoid electrical damage, always power off the SUT before cleaning the compression footprint.*

The following procedure is recommended to obtain best performance.

Clean the compression foot prints on the circuit board of the SUT before connecting the probe.

1. Use a lint-free, clean-room cloth lightly moistened with electronic/reagent grade isopropyl alcohol, and gently wipe the footprint surface.
2. Remove any remaining lint using a nitrogen air gun or clean, oil-free dry air.

Install the probe retention assembly

The probe retention assembly provides a single-piece housing around the connector footprint to help stabilize the probe.

To install the probe retention assembly on the circuit board, do the following:

1. Locate the correct footprint on the SUT. If you intend to use multiple probes, your PCB has multiple footprints. Be careful to select the correct one.
2. Clean the compression footprint as described above. (See page 37, *Clean the compression footprints on the SUT*.)
3. Align the retention assembly over the footprint so that the keying pin on the retention assembly lines up with the keying pin hole on the footprint.

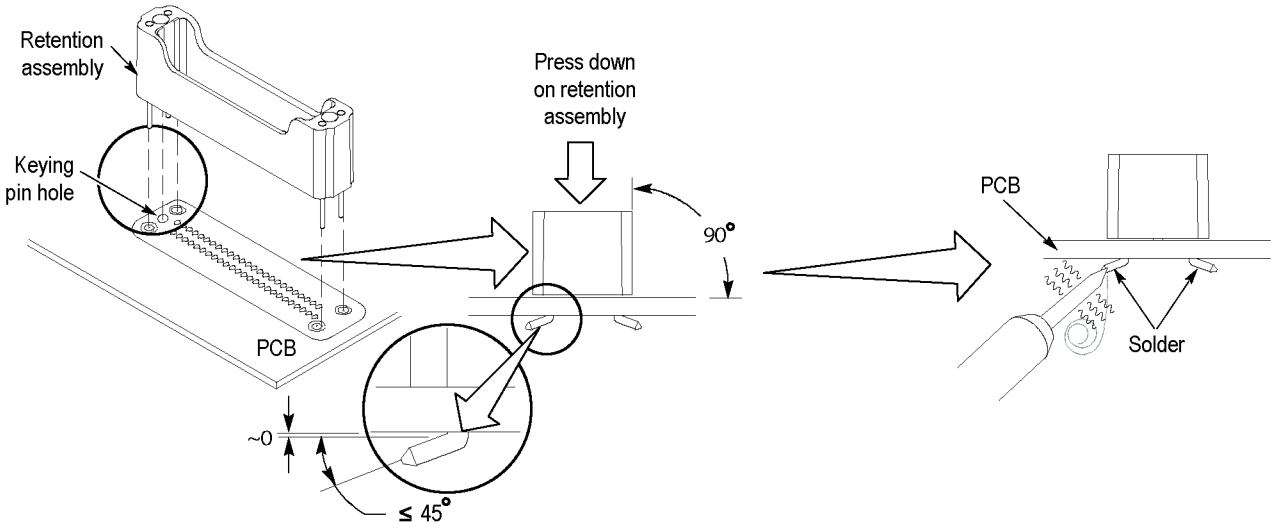


Figure 25: Installing the probe retention assembly

4. Insert the retention assembly into the holes in the footprint on the PCB.

NOTE. *The following two steps are important to be sure that the retention assembly is correctly mounted and that the probe makes proper contact with the PCB.*

5. Hold the retention assembly so that it is firmly flush with the surface of the footprint, and the four anchoring posts extend through the circuit board to the opposite side.
6. Using a pair of needle-nose pliers, hold one of the posts. Using the circuit board hole as a fulcrum, bend the post outward so that it is flush with the PCB surface, anchoring the assembly to the PCB. Bend the other three posts in the same manner.
7. Solder the anchoring posts to the PCB.

Retention post information

The retention posts are available as on optional accessory kit (Tektronix part number: 020-2539-xx). The retention posts are mounted on a plastic carrier for easy installation to the PCB. Two lengths of wire are shipped with the posts to allow use with thicker PCBs.

If the PCB is less than or equal to 0.120 inches thick, use the wires that come preattached to the posts. If the PCB thickness is greater than 0.12o in., use the longer wire that is included with the posts. The longer wires are embedded in the protective foam of the retention post kit.

Replace the retention post wires

Perform the following procedure to replace the shorter retention post wires with the longer wires:

1. Remove the old wire by pulling the side of the wire over the retaining tab and lifting the wire away from the post.
2. Place the new wire in the slot side without the tab, and then wrap the wire over the tab side until it engages in the slot (you will feel or hear a slight click).

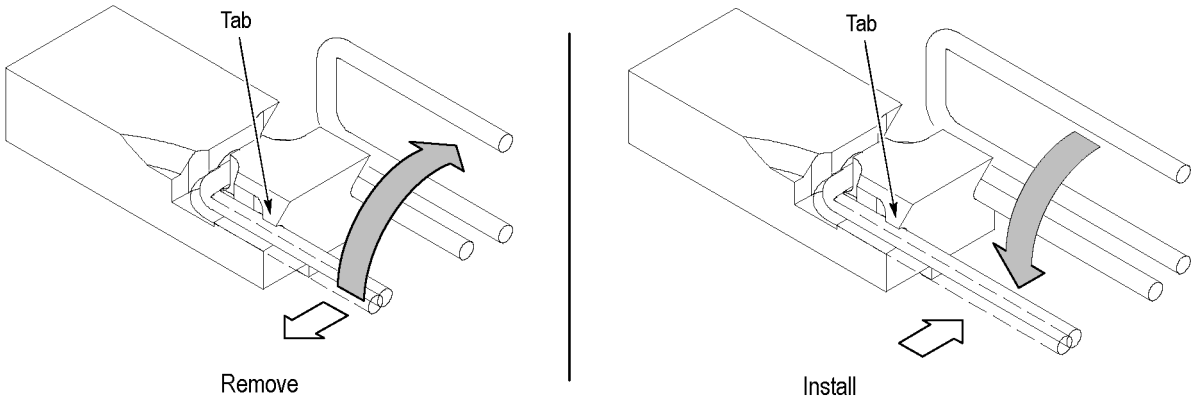


Figure 26: Replacing the wires on the retention posts

Install the retention posts on the PCB

To install the retention posts on the PCB, do the following:

1. On the retention post/carrier assembly, locate the black retention post (the post with the keying pin) and align it to the keying pin hole on the PCB. (See Figure 27.)
2. Press the retention posts into the holes on the footprint on the PCB.

NOTE. *The following two steps – bending and soldering the wires to the circuit board – are the two most important steps in assuring that the probe retaining posts are correctly mounted. Bending the wires before soldering them helps prevent long-term cold solder flow.*

3. Press down on the carrier and bend the post wires out to anchor the posts to the PCB. Ensure the assembly is perpendicular to the PCB when bending and soldering the post wires.

   The bend point in the retaining wire should be as close to the circuit board surface as possible. Grip the wire with a pair of needle-nose pliers about 1/8-inch above the circuit board surface and let the side of the through-hole (not the pliers) act as the fulcrum point for bending the wire. This method pulls the probe mounting posts tightly against the circuit board surface.

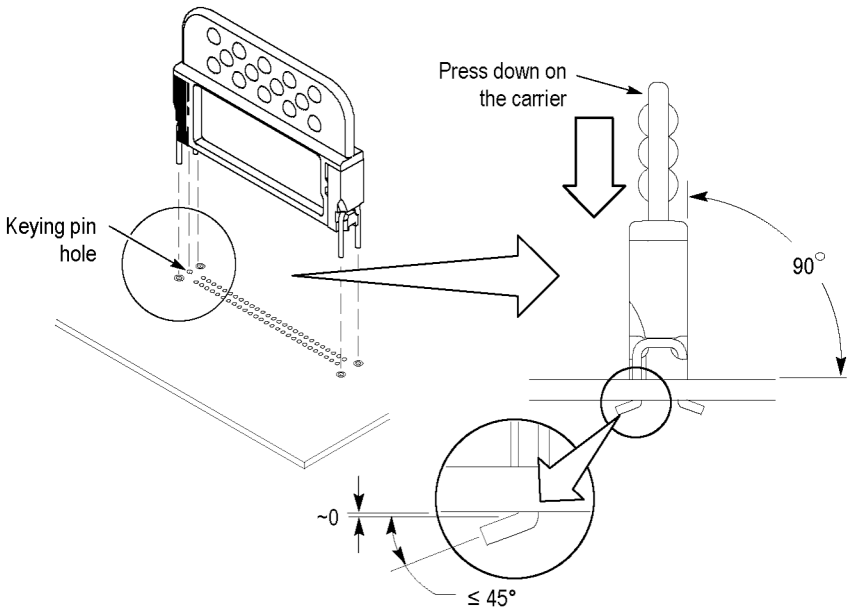


Figure 27: Installing the retention posts on the PCB

4. Solder the posts to the PCB. (See Figure 28.) The posts can be soldered from the top or bottom of the circuit board, but it is best to solder the bottom to avoid the heat-sinking effects of the posts on top.

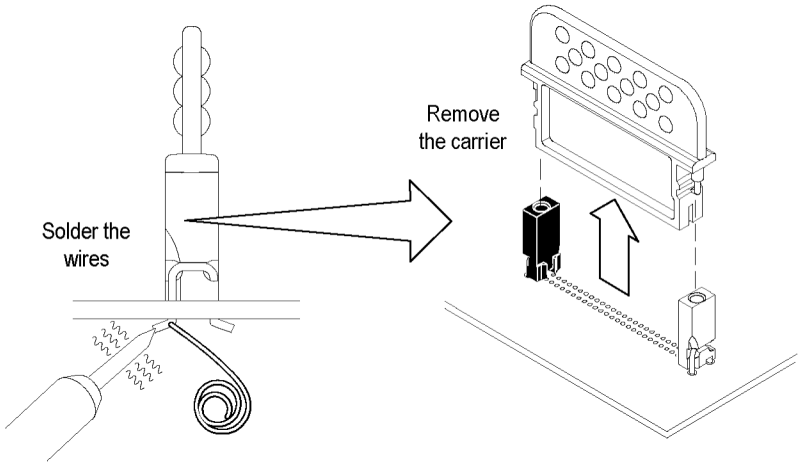


Figure 28: Soldering the retention posts on the PCB

5. Pull off the carrier from the posts.

NOTE. *The posts may have a small amount of movement after you solder them to the circuit board. This is normal and accounted for in the post design.*

The probe should mate firmly to the board when the two screws are tightened to the mounting posts. The screws have a mechanical stop on them to prevent over-tightening the probe to the board.

After a probe has been installed and removed, there may be slightly more play in the posts. This is also normal and accounted for in the probe design.

Glossary

cLGA

An acronym for compression Land Grid Array, a connector that provides an electrical connection between a PCB and the probe input circuitry.

Compression footprint

A connectorless, solderless contact between your PCB and the P5960 probes. Connection is obtained by applying pressure between your PCB and the probe through a cLGA c-spring.

D-Max probing technology

The name that describes the technology used in the P5960 high-density logic analyzer probe.

Functional check procedure

Functional check procedures verify the basic functionality of the probes by confirming that the probes recognize signal activity at the probe tips.

Keep out area

An area on a printed circuit board in which component, trace, and/or via placement may be restricted.

Logic analyzer-end

The end of the probe which connects to the logic analyzer.

PCB

An acronym for Printed Circuit Board.

Probe head

The end of the probe that connects to the SUT.

SUT

System-Under-Test. Also known as the target system. The logic analyzer connects to the SUT through the probe.

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